

**U.S. Patent Application Serial No. 09/351,544**

**Declaration of Timothy K. Carns**

**Document C**

---

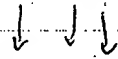
- Arrive work @ ~8:12am

- Read emails

- Start working on the PEVAL data / summary again for D1114.

Nplus

NPCONTY1



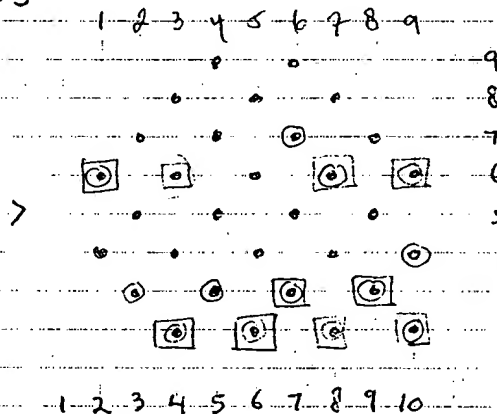
Serpentine  
continuity

NPBRI01

= Vt f pnc



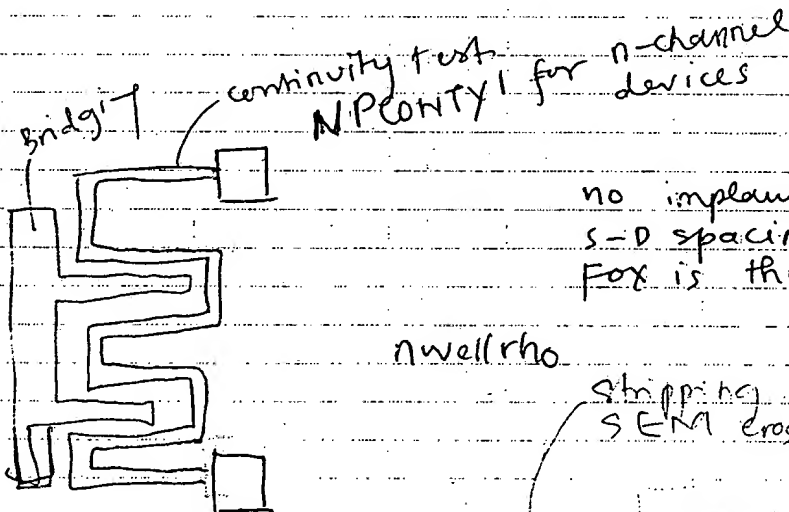
D1114-3



pt source drain

○ - wfr 3

□ - wfr 4

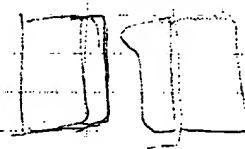


no implant  
s-d spacing is low  
Fox is thin

nwell rho

stripping back (top down)  
SEM cross-section

wfr 13 & 14



PT bridge &  
continuity structure  
Ask Scott

gate is shorted to S-D

problem will probably not be solved  
look at PEVAL data more carefully.

7365  $\rightarrow$  237235

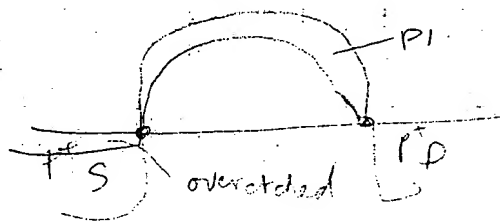
4. ~~K16~~ K16 lots of room than L02 (3x3)

~~more~~ smaller die  $\rightarrow$  more scribe we have

Talk Scott - Layout structure, design violation

- BVDSFPP, LK GFPP look ok

- overetch P1 (L40)



if there is a layout problem, then we should see it more often

not a self-align gate, because it is a field device

pt diffusion

diffusion to diffusion ~~is~~ is not violated

$3.5 \mu\text{m} = \text{min diff-diff space to get Fox in there}$   
 $0.875 = \frac{3.5}{4}$

$0.875 \mu\text{m} = \text{minimum diff-diff space to get Fox between S \& D}$

compensate (0.5  $\rightarrow$  0.35  $\mu\text{m}$ ), no design violation

2.5      0.8      1  
1      1  
270      260      2-50

$V_D = 3.3 \text{ V}$  , 3.5 V (max)

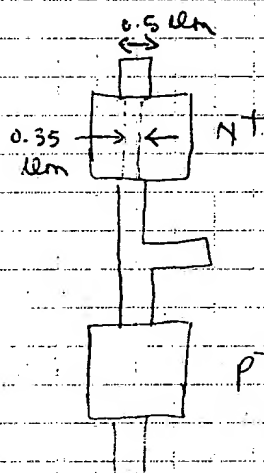
max potential of S-D

CMOS CMOS  
7223 = 7120

7235, well  $V_t$  implant is modified  
well Punchthrough

$T_{gate\text{-}ox} = 70 \rightarrow 110 \text{ \AA}$   
E37235

min poly line width  $\uparrow$  from  $0.35 \rightarrow 0.5 \mu\text{m}$



E36223 & E37223, the  $N^+$  device, the  
gate width is drawn  $0.5 \mu\text{m}$ , but  
in the fab it is compensated to  $0.35 \mu\text{m}$ .

The  $P^+$  device's gate width is NOT  
compensated.

In E37235 device, Both  $N^+$  &  $P^+$ 's gate width =  $0.5 \mu\text{m}$ .  
They will not be compensated. What you see is what you  
get.

Field,  $V_D = 5V$   
NMOS,  $V_{DS} = 3.5V$  (max)

$$\frac{3.5 \mu\text{m}}{4} = 0.875 \text{ - diff. to}$$

Unless they are same pot  
& same rate

unrelated diffusion



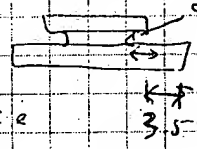
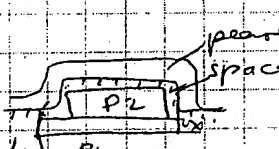
Capacitor Etched meeting 2pm : PI & UPD & M groups  
~~Meeting 2pm~~

Show D1261 has good capacitor but other problem arises  
Swing effect that PEARL had fixed, & now can not be fixed

### Problem Avoidance

1. too many steps
2. redeveloping "
3. Don't recreate cap. leakage & yield sensitivity big sigma.
4. Do we want technician to distinct 737120 vs 7223 flow

### Solutions:

- ① Don't remove <sup>inter poly dielectric</sup> IPD at L39 "punch it" at L40, 1168, 1549. Lot
- ② Wet (50:1 BOE) IPO Removal at L39 has 50% overetch  

3. Use 4528 dry removal w/ L39 in place w/ or w/out resist in place
4. Flow layer 39 resist / Build more polymer / 1 mask (no budget to buy)  
we have etched tech to do this
5. BARC (needs a lot of development)  $\Rightarrow$  use it as back burner
6. If oxynitride (PECVD) then potentially = PEARL (1168 ~~1549~~ Lot)  
as the dielectric layer. Want to analyze 1168 lot before considering this option.
7. Return to the 6223 flow (-)
- ⑧ Seal edge w/ RTP or Dep/spacer etch  

9. Use IPO as "ARC layer" (nitride / pearl / etc)
10. multilayer ARC (nitride / pearl / etc)

Is it pearl between the poly plate or pearl

Leaving oxide under pearl is not going to work.

Swing effect  $\gg$  big  $\sigma$

Questions what are the experimental questions that need answer

1. Leakage path due to oxide undercut, P2-pearl-P1 or P2-undercut - P1

2. quantify impact to BPSG CMP & contact etch.

3. what is  $\sigma$  difference for various conditions, vs. psc.  
IPO or ARC

4. Cost & complexity (near & long term) comparability to E37223)

5. Are CMOS XTR's still happy

6. Meet all other measurables per psc (roll-off)

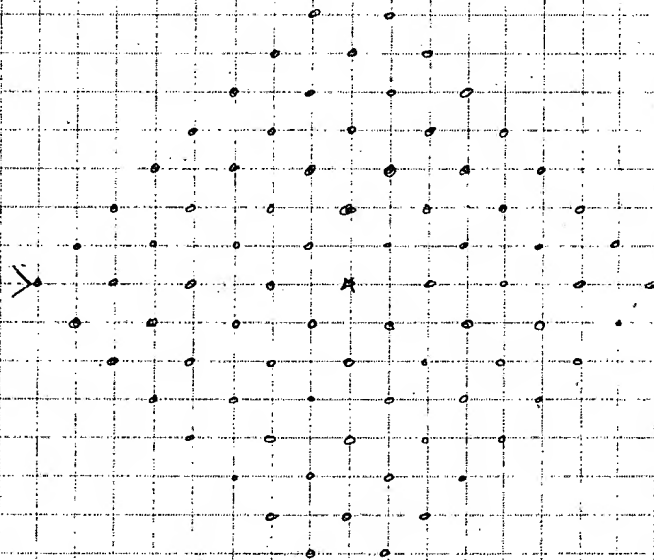
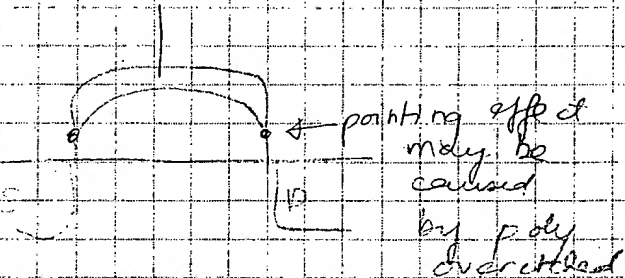
<u>Factor</u>	<u>Action / Levels</u>
* Pearl	Y N Thickness
* IPO Removal (L39) from transistor	Wet, dry, polymer, LE Mask, not doing anything
* Edge Seal (method / thickness)	RTP, Spacer (deposition & spacer etch) <sup>1000 vs 2250 °A</sup>
* IPO Material	Thermal, dep-oxide, dep ox, grow / dep $\text{OH}_2\text{O}$
* L40 Exposure	A way / splits

Don't need waffles toward BPSG polishing

what have been done in D1168, D1261A & D1549 lots to narrow down these possibilities

poly overetched

→ cause  $V_{thppc}$  to shift dramatically in D1114 (Summary report)



- Arrive work ~ 11:30 am

- Work on D1114 PEVAL Summary report

- Got most of Rm done, except in Executive Summary & the poly-overetched stuff (w/waffles) that may caused the field poly gate defects at/near the S/D ( $I_g \gg I_d$ )

- Left ~ 9:50 pm

12/14/98, M

- Arrive work ~ 8:10 am

- Attend the 8:10 meeting → 8:35 am. J. Smythe mentioned that L-40 mask WITHOUT WAFFLES would be here today

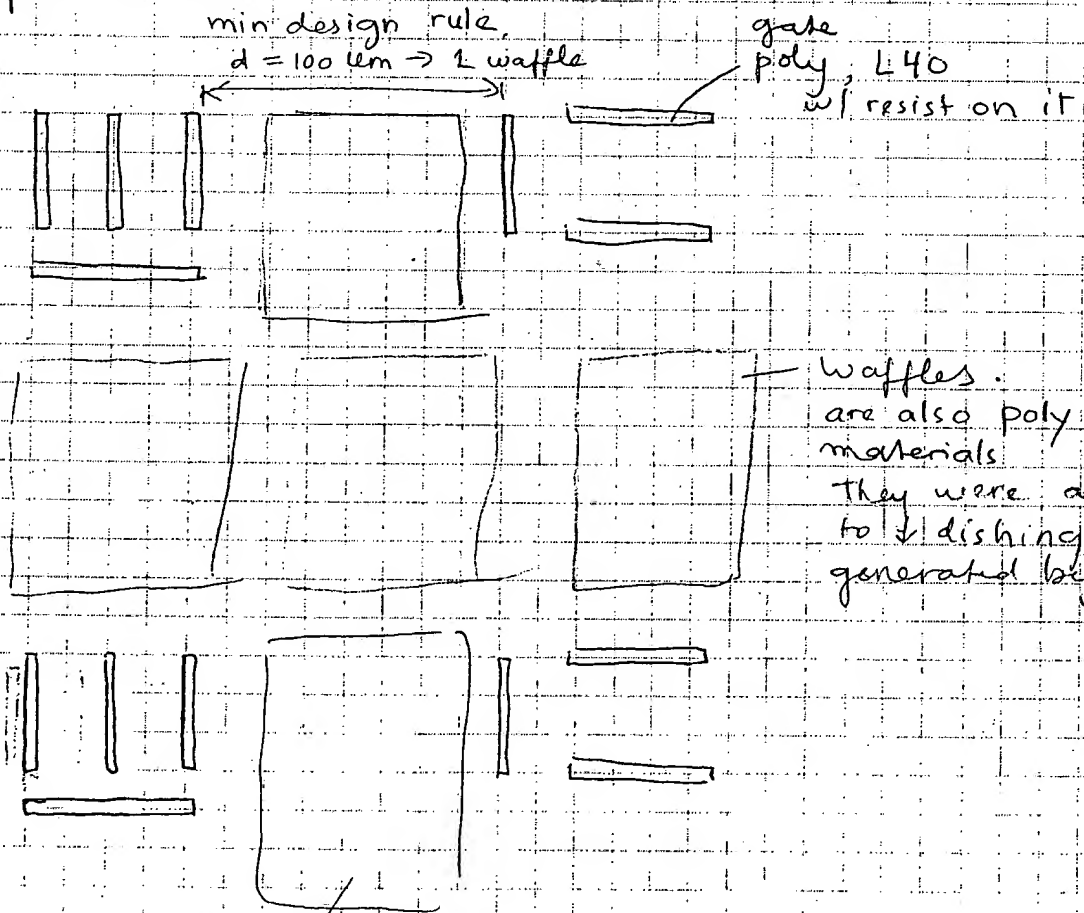
- Call US West to pay bill \$53.86 (not paid \$ ~67. from budget call)

- Read emails → print out the email from John Smythe about the discussion on

- Work on DIII4 PEVAL Summary report.

- Talk to Mike about overetch poly 1 (L-40) caused by putting waffles in the open / unused area to reduce the dishing from polishing (CMP)

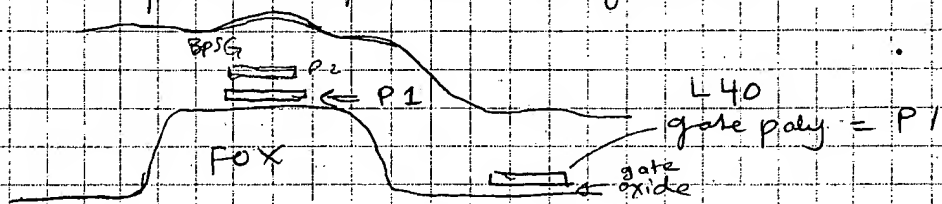
In standard / normal Z-70 process, there is a lot of open area:



Cover w/ resist  
at L-40 etch

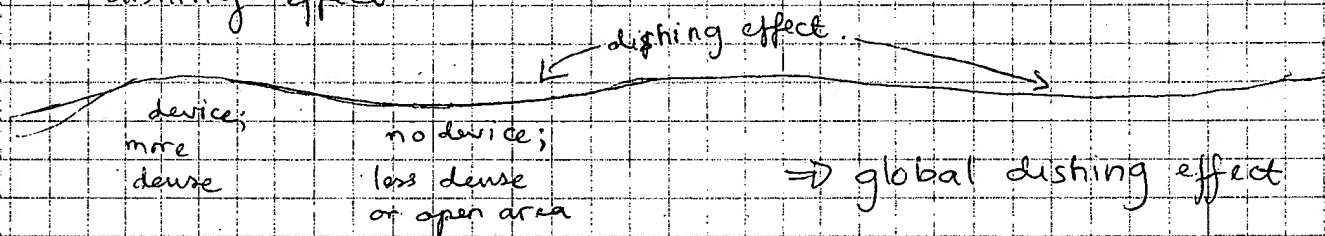


The previous picture is equivalent to:



As you can see that without waffles, a lot<sup>of</sup> poly will get removed @ L-40 etch. Typically 90% or more poly got removed.

Also without waffles, when polishing the wafer after BPSG 1 was deposited, the open / less dense area gets polished faster & deeper than the more dense area. This uneven polishing rate creates the so-called a dishing effect.



This dishing effect can cause problem for leaving an unnecessary layer of metal on a device, i.e., metal (W-plug) may not be removed completely, etc.)  $\Rightarrow$  cause shorted device.

So, decision was made to add WAFFLES in the area where there is open area of 100  $\mu\text{m}$ . Design rule is to add a waffle where the gate poly are at least 100  $\mu\text{m}$  apart (100  $\mu\text{m}$ , 200  $\mu\text{m}$ , 300  $\mu\text{m}$ , etc.)

Waffles were added to reduce dishing effect.

So now w/ waffles (= poly gate metal), the <sup>total</sup> amount of poly gate removed at L-40 etch would be much<sup>2</sup> less than there is no waffles.

With tremendously smaller amount of poly to be removed, there is so much reactive gas left in the chamber to continue etching the area not covered by resist.  $\therefore$  Poly etched rate is much faster & thus deeper.

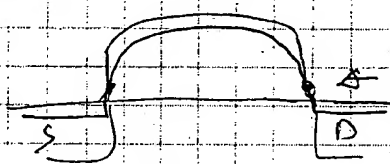
This faster etch rate, etch right through the gate oxide & attack the single crystal underneath it.

That's why we trench the substrate in lot D1114.

The entire problem is caused by NOT adjusting the amount of reactive gases in the chamber w/ smallest amount of poly gate removal.

Obviously, there is an etch rate difference for more vs. less dense area that can cause non-uniformity throughout a wafer. Typically, more dense area etched slower than a less dense area.

= Add the above discussion to D1114 lt report to support the large shift of VTFPPC that was thought to be caused by the field edge defect of poly gate & <sup>possibly</sup> caused by over etched poly gate to trenching the substrate.



high field  
trench into substrate  
caused by over-etch poly gate  
in D1114

- Got the report done ~12:30 pm, make copies & arrange the appendices. Go to lunch  
the report
- Gave to Mike ~1:30 pm. Ask Mike about the next priority. He told me to look at / think about what kind of split we can do (on top of D1261, D1168 & D1549) that can answer the problems / questions addressed on meeting.
- Ask Mike & Lee of the 1261, 1168 & 1549 split lists, go make copies
- Send a package out → go to shipping & handling.
- Around 2:15 pm, go to Bldg 1 to pick up the software for remote access from Armand Sermonia. He showed how to access my emails & MS's application a little bit. Make copies on the procedure to install the software.
- Back to Bldg 2, send out emails to Brett Lowe to see if he is going to SL. He is NOT.  
Talk to Donna about the power off on 12/29/98 whether decision has been made as to let us take a vacation on that day or use as substitute. No decision is made yet.  
Tim is in - Israel the whole week.  
So, I emailed Din informed him of the off day @ Zilog on 12/29. May need to arrange my traveling plans.

- Look at the split list of D1261, D1168 & D1549. Try to make some sense why certain splits were done.
- This is my next project to see how we can answer the questions addressed on <sup>meeting</sup> about the alternative cap-ox mix, capacitor leakage & etc. In general, about finding a process that would be best for both transistor & capacitors.
- Wafers 13 & 14 from D1261A lot received thermal capacitor oxide twice, because the cap-ox strip step didn't remove all of the oxide. (#1 step run card has wrong recipe name on it).

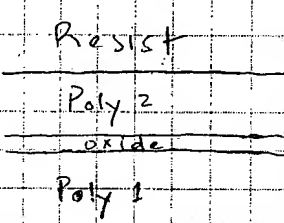
- Leave work ~ 7:05 pm.



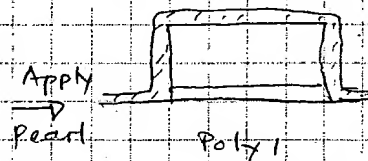
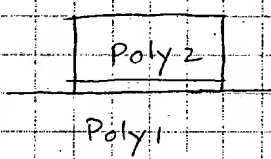
12/15/98, T

- Arrive work ~ 8:10 am
- No mails
- Read Industry news distributed every Monday
- Read the printout from John Smyth about the

} } } UV

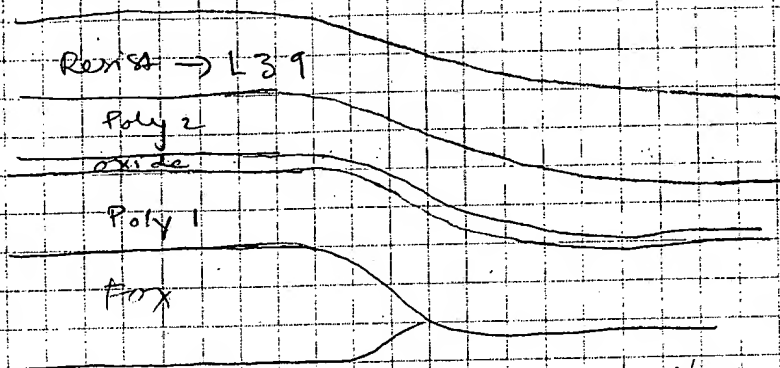


- pattern (L39)
- etch
- remove resist

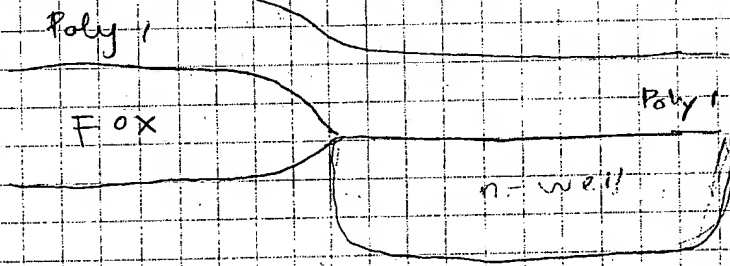
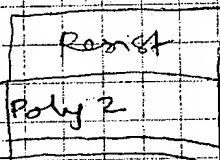


Pearl layer  
is directly on top  
of poly 1  $\Rightarrow$  give good  
CD control  
of L40 exposure

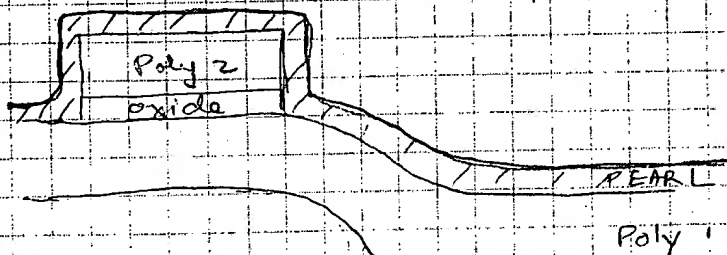
D1114: (Initial L39 & L40 etch)



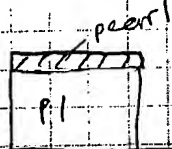
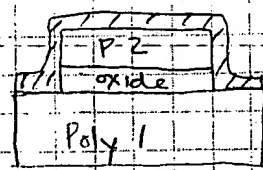
- exposed resist w/uv
- pattern L39 (P2) dry etch
- etch P2 & IFO (inner poly oxide) removal using
- wet etch tech. The wet etch is used to remove oxide only.



Remove Resist  
↓  
deposit ARC or pearl layer



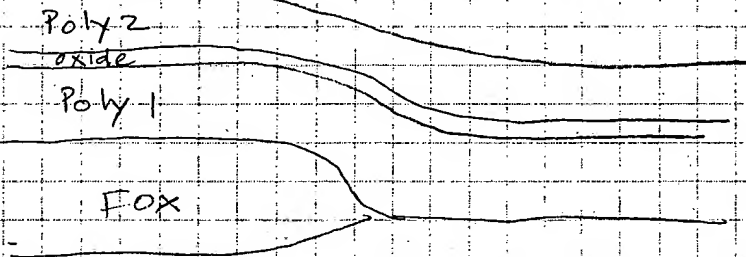
Apply Resist for L40 (P1) pattern



WITH PEARL directly ON top of poly 1 → better / good control of CD @ L40 mask

L39 & L40 etch proposed by John Horvath.

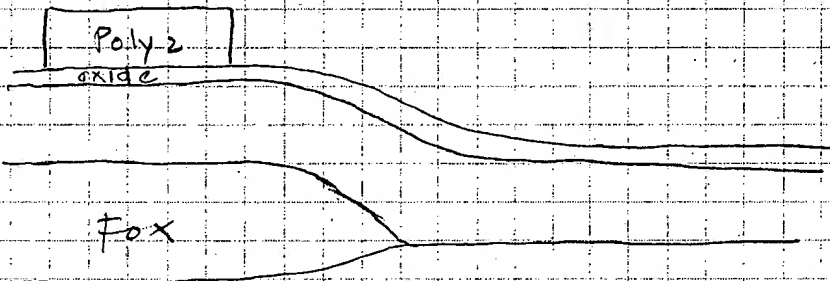
Resist for L39 pattern



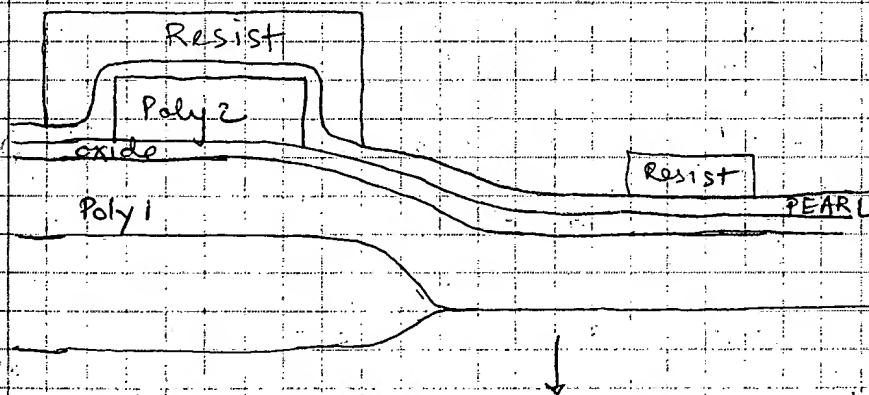
L39 → Poly 2

L40 → Poly 1

↓ Dry Etch Poly 2 ONLY  
↓ Remove resist

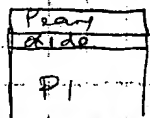
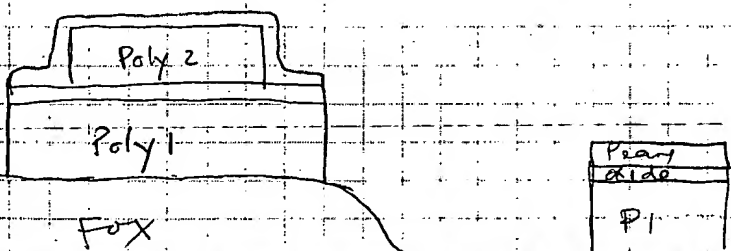


↓ Deposit PEARL  
↓ Apply Resist to pattern Poly 1 (L40)



THEY CLAIMED that  
w/ PEARL ON TOP of  
OXIDE instead of  
poly 1 resulted in  
poor CD control  
@ L40

(As J. Smythe put it:  
Loss in swing suppression  
at L40 mask)



ARC = Anti Reflective Coating

PEARL = Plasma Enhanced Anti Reflective Layer

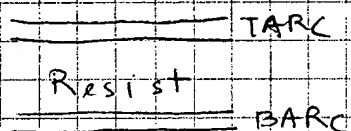
Oxynitride, ONO

ARC = PEARL or pearl is part of ARC

ARC can be \* organic (contains Carbon) (can be removed)  
\* inorganic (TiN, oxynitride or nitride) (can not be removed)

BARC = Bottom ARC

TARC = Top ARC



ARC is a generic term

PEARL is the trade-mark name of Novellus film  
PEARL is used to improved line-width of photomasks  
(better control of line-width)

PEARL is Si-rich w/ some oxygen & Nitrogen.

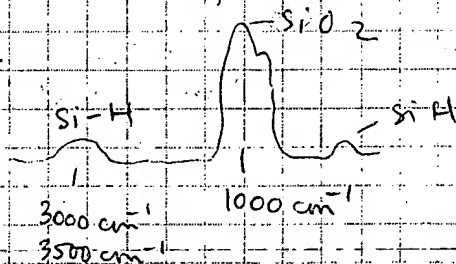
PEARL  $\Rightarrow$   $\text{SiO}_x\text{N}_y$  (Si-rich),  $\text{SiO}_{1.99}\text{N}_{1 \rightarrow 1.2\%}$

I've talked to Jim Shau, Brett Lowe & John Smythe; no one can tell me what the pearl composition is.

Typically (@ Zilog), PEARL is deposited using a PECVD.  
Although thermally grown PEARL is also possible using LPCVD (Low pressure chemical vapor deposition) tube at  $\sim 650-700^\circ\text{C}$ ?

Pearl has refractive index:  $n = 2.4$  &  $k = 0.5 \Rightarrow \therefore$  Both  $n$  &  $k$  are important

FTIR



Si-H is observed when there are dangling bonds

$n = 2.3$  (@  $\lambda = 633\text{ nm}$ , expose @  $365\text{ nm}$ ). This is the only  $\lambda$  that they can measure  $n$

$n = 2.3$  (@  $633\text{ nm}$ )  
 $n = 2.53$  (@  $365\text{ nm}$ )



$n$  will tell you how fast the light passes thru a medium  
 $k$  is absorbance / loss

$n + ik$

Pearl is typically deposited @ 13.6 MHz (high frequency)  
The Novellus system can only operate at this frequency.

Oxynitride is deposited using the same chamber  
as PEARL  $\Rightarrow$  PECVD. But the gas ratio of  $\text{SiH}_4$ ,  $\text{N}_2\text{O}$  &  $\text{NH}_3$  are different.  
using both high (13.6 MHz) & low (20-40 MHz)

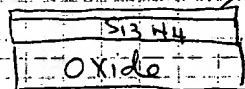
Oxynitride is NOT rich in Si, it is a natural IPD  
(Inter Poly Dielectric). From the name, oxynitride, I wonder  
if it rich in oxygen & nitrogen?

It contains  $\text{SiO}_x\text{N}_y$ , it is a one layer of  $\text{SiO}_x\text{N}_y$ .

$n = 1.75$  &  $k \approx 0$

Oxynitride can also be thermally grown using LPCVD tube  
at  $\sim 650 - 700^\circ\text{C}$

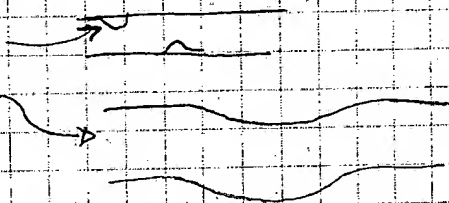
ONO = Oxide, Nitride, Oxide  $\Rightarrow$  3 layers of film  
 $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{SiO}_2$



oxide (much thinner because oxidation  
rate of ~~Si~~ Si from  $\text{Si}_3\text{N}_4$  is  
much harder)

Without Pearl, when a material is going thru a photolithography step, we see:

- reflective notching
- thin film interference



In general w/o pearl  $\Rightarrow$  non-uniform layer after exposed

WITH Pearl, the above optical problems were reduced  $\Rightarrow$  more thickness uniformity

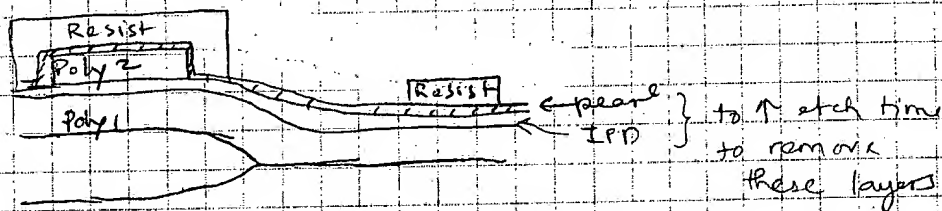
- Ask Mike about the notes - several words/terminology

IPM = Identical Process Module

SPM = Similar " "

Loss in swing suppression @ L40 mask  $\Rightarrow$  poor CD controlled

$\uparrow$  Length of punch-through step in L40 to account for PEARL + IPD  
=  $\uparrow$  the etch time



Mike also mention, typically it takes a lot of justification to add an extra masking. Yet in the "Comparison of Approaches by Step" (note from Smythe) indicating that there is a new mask level for the under-exposed L39. About 4-weeks ago when the new mask was proposed, most people against it & prefer the J. Horvath etch proposal; yet it looks like now Tim & John S. do not want to use Horvath etch tech, but want to do s.t. else.

Leave ~ 6:20 pm

The transistor & capacitor from D1261 lot look great. D1261 used J. Horvath etch proposal to etch L39 & L40.

12/16/98, Th

Arrive work around 8:12 am

Read & response emails

I'm going to start doing the split list based on the discussion or meeting we have

The last couple days I have been looking over the split list done on D1168, D1549 & D1261A to see what we are trying to accomplish by doing that splits, hopefully to not redo it again.

87L02

\* Split list of D1261A for Capacitor Oxide Etch :

Wfr #	Cap. Oxide	Cap. Ox Etch	L40 - Expo Split	L40 Etch	Hook
11	Thermal	BOE	Yes	D1114	D1114 w/ 2
12	—	BOE	Yes	GOLD	
13	—	Horvath	"	Z7223L40	
14	—	—	"	Z7223L40	
15	—	—	"	Z7223L40	
16	Novellus	BOE	"	D1114	D1114 w/ 4
17	Novellus	BOE	"	GOLD	
18	—	Horvath	"	Z7223L40	
19	—	—	"	—	
20	—	—	"	—	

Wafers 14 & 15 received thermal oxide twice because the one step runcard had the wrong recipe to remove the capping oxide ( $\Rightarrow$  not all oxide of removed)

D1261A didn't receive L40 DCD splits on a wafer. However, the PEVAL data show that we have data down to roll-off region. According to Mike, it is the different etching at L40 causes different  $\leftarrow$  off. (Maybe not enough polymer to protect the nearby surrounding)

\* Split list of D1549 capacitor oxide Etch:

wfr	Cap. Oxide	Cap. Ox. Etch	L40 D1CD split	L40 Etch	L50 Etch	Hook
1, 11	Thermal	BOE	Yes	D1114	D1114	D1114 wf. 2
2, 11	— " —	BOE	Yes	GOLD	D1114	
3, 13	— " —	Horvath	Yes	Z7223L40	Horvath	
4, 14, 21	— " —	— " —	No	Z7223L40	— " —	
5, 15, 22	— " —	— " —	No	Z7223L40	— " —	
6, 16	Novellus	BOE	Yes	D1114	D1114	D1114 wf. 4
7, 17	— " —	BOE	Yes	GOLD	D1114	
8, 18	— " —	Horvath	Yes	Z7223L40	Horvath	
9, 19, 23	— " —	— " —	No	— " —	— " —	
10, 20, 24, 25	— " —	— " —	No	— " —	— " —	

The split lists of D1261 A & D1549 are very similar, except the additional split on L50 etch for D1549.

From these 2 lots, if everything runs as it should be, we should be able to distinct the following:

\* Thermal vs. Novellus

\* Buffer Oxide Etch (BOE) vs. Horvath Capacitor Ox. Etch at L39 <sup>wet etch for IPO removal at L39</sup>

\* L40 D1CD splits on a wafer will determine roll-off

\* L40 etch (D1114, GOLD & Z7223L40) may still need to be optimized as they seem to shift the <sup>most of</sup> left outside the spec window =  $0.33 \pm 0.05 \text{ } \mu\text{m}$

\* The L50 Etch (D1114 & Horvath) in lot D1549 may also need optimization (no PEVAL data yet at this point). But L50 etch splits were added in D1549 to take into account longer / higher <sup>rate</sup> etching for having Pearl & IPO on poly 1.



\* Split List for D1168 is too much work to list. So, see the original split is. Except wfrs 8 & 16, the rest of wafers receive no IPO removal at L39 (Horvath etch).

Again, if everything is going ideally, then we should be able to differentiate the following:

\* Thermal vs. Novellus ONO Bottom Oxide ( $320^{\circ}\text{A}$ )

Thermal vs. Novellus hook back to D1114 (wfr. 8 & 16)

\* Using oxynitride as IPD vs. ONO & Oxide

\* For Novellus Bottom oxide : (a) WITH TOP ONO oxide vs. WITHOUT TOP ONO oxide

wfrs - received thermally grown top ONO oxide : (b) time & temp ( $850^{\circ}\text{C}$  &  $970^{\circ}\text{C}$ )  
(10 min vs. 176 min)

\* For Thermal Bottom ONO oxide :

(a) With Top ONO oxide vs. NO top ONO oxide

(b) wfrs that received thermally grown TOP ONO oxide:  
time (10 min vs. 176 min) = 5224 process @  $970^{\circ}\text{C}$   
temperature ( $850^{\circ}\text{C}$  &  $970^{\circ}\text{C}$ )

\* For Oxynitride IPD (all have  $530^{\circ}\text{A}$  thick) :

(a) WITHOUT vs. WITH TOP ONO OXIDE. The wafers that received top ONO thermal oxide @  $850^{\circ}\text{C}$  for 10 mins will be tested because of this extra thermal cycle.

(b) Annealing after oxynitride deposition (wfrs 17-25) & thermal top ONO oxide (wfrs 19, 21 & 23); distinct different annealing condition:

$40\% \text{N}_2\text{O}$  TVFO1 (tube) @  $850^{\circ}\text{C}$  - 10 min vs.  $\text{N}_2\text{O}$  RTP @  $1050^{\circ}\text{C}$  for 40 min. vs.  $100\% \text{NH}_3$  @  $850^{\circ}\text{C}$  for 10 min

\* L40 D1CD split  $\rightarrow$  roll-off analysis.

\* Generate the split list  
Divide the split list from J. Smythe into 5 splits

### Comparison of Approaches by Step

Approach Number	Ox	Ox	Ox	Ox	Ox	Ox	Ox	Ox	OxNit	ONO	ONO
IPD Material	X	X	X	X	X	X	X	X	X	X	X
Poly 2 Dep	X	X	X	X	X	X	X	X	X	X	X
Poly 2 Imp	X	X	X	X	X	X	X	X	X	X	X
Poly 2 Anneal	X	X	X	X	X	X	X	X	X	X	X
Deglaze	X	X	X	X	X	X	X	X	X	X	X
L39 Mask	X	X	X	X	X	PMR	PMR	X	X	X	X
L39 Poly Etch	X	X	X	X	X	B/D	B/D			DO	
L39 IPD Removal	B/D	B/D	B/D			X	X	X	X	X	X
L39 Resist Strip	X	X	X	X	X	X	X	X	X	X	X
New Mask				UE	UE						
IPD Removal				B/D	B/D						
Resist Removal				X	X						
Spacer Oxide		RTP	DEP	RTP	DEP	RTP	DEP				
Spacer Etch			X		X		X		Y/N	Y/N	X
PEARL Dep	X	X	X	X	X	X	X	X	X	X	X
L40 Mask	X	X	X	X	X	X	X			X	X
L40 Etch	X	X	X	X	X	X	X	PTD	PTD	X	PTD
	#1			#2		#3		#4		#5	

B=BOE, D=DRY, UE=UnderExposed L39 mask; PMR=L39 etch with added OE polymer;  
PTD=L40 etch with punch through increased for IPD+PEARL; Y/N=WITH/WITHOUT;  
DO=Dry ONO etch

Combine Splits 1 & 3; split 2 & 4; split 5

If we actually going to do all of these splits, need to know the following:

Split 1 & 3 :

SDE = Statistically Design Experiment

for LB9/L40 on 87L02

This is actually what my project is called → to do the split list stuff.

Go over the split list w/ M. Westphal. There are a few suggested changes: Horvath → actually L39 resist strip only  
Add the hook wafers #

~ 5pm → 5:30pm

Send out those split list (capox-split 3, capox-split 2+4 & capox-split 5) to Mike, John & Tim. This is what I say in the email:

Attached are the proposed splits for L39, IPO, L40 RT on 87L02 based on the table below (J. Smythe). I group the table into 5 major splits. Split 1 = the 1st 3 columns (reading from left to right), split 2 = col 4 & 5, split 3 = col 6 & 7, split 4 = 8 & 9, & split 5 = col. 10 & 11. It looks like 3 lots will be sufficient to do all splits.

Feel free to make comments & suggestions on the proposed splits & let me know of any changes you would like to see.  
Thank you.

This email was sent out around 6:38pm.

Leave work around 6:45pm.

Go to Albertson's directly to buy some ribbon or bows & cards, but couldn't find a good deal. So I went home to have my dinner & then went out again to Paul's grocery store to buy those items.

Making cookie dough from ~ 9pm → 12pm.

12/17/98, TH

- Arrive work at 9am. Pretty tired so I woke up late from making cookies dough last night
- Let Donna Lowe know (~8:20 am) that I'm going to be late.
- Talk to Mike about what I should do next. Nothing much.
  - He told me to go ahead send out a meeting notice to every-one to discuss the split list for 87L02.
  - so I did
- I tried to log in to WHITE to learn how to create a new STR. I was not successful.

- Might want to ask Scott about the status of IDC for me to analyze (do manual measurement) on the new SLM of 87L02 (Z37223).

Last several SLM meetings were focused on new SLM that can be used for double (Z27223) & triple (Z37235) layer metals.

- Send out Christmas card for Tim, John & Pete
- Will bring cookies to Donna, David, Lee, Mike, Thomas, Scott, Amin, Shawn, Bee, Deb Auck, Jean & Margurit, Min, Jim & ~~Karen~~ tomorrow
- According to Mike that we are still waiting for D1168 & D1315 PEVAL data. So there is not much to do.
- ▽ - The meeting notice was sent out to: John Esposito, John Horvath, John Gold, Brett Lowe, Mike Westphal, Steve Buffat, Jon Daley, Lee Debruler, Thomas chung, Bee Kickel, John Smyth, Tim Lams, Min Huang & Alan VonKrosigk.  
The meeting will be tomorrow at 10am in Blue Room
- Think about why certain splits were proposed, how the previous splits (D1261, D1168 & D1549) can answer some of the questions (so no redundant will be done hopefully), how the current splits can answer those questions as well.



- see a doctor from 1:30 → 3pm. Have to argue w/ them that I have an insurance, even-though I don't have the card yet. Dr. Asadorian wants me to set up an appointment w/ a physical therapy. I called the physical therapy office, have an apt at next Tuesday at 8:15am at the MOST Therapy center nearby Mercy Hospital

- Rest of afternoon play w/ generating a new STR.  
Called up Wendy on how to log-in.  
Get most of help from Mike while Thomas watched us.

- Asked Mike what I should do for the meeting tomorrow

- ~~Amatt~~

12/18/98, F

- Arrive work ~ 8:05 am
- Distribute christmas goodies till around 8:25 am
- Back on looking at the proposed split lists & thinking how to present them at 10 am meeting.
- Mike came talk to me and tell me to spare the details (i.e. of thinking the split lists).
- Shawn came talk to me about the topic: why when we already knew that wet etch causing an undercut of oxide below P2. I don't know how he knew. My guess is Mike might have told him <sup>that's fine</sup> & told him to come talk to me so I get some-kind of practice before the presentation.
- Meeting at 10 am to review the split list.  
Jon Daly, Bee Kikel, John Esposito, John Gold, Brett Lowe, Jim Shaw, Minn Huang, Lee Debruler & Mike Westphal attended the meeting.

John Smythe didn't attend even though he accepted the meeting invitation. I went to look after of everybody in Blue room waiting for him. he was not at his office, so I asked operator to page him. Later Donna came told us that he is bldg #1 w/ Dale Manos to meet w/ Mike Bradshaw. They were there from ~ 9:45 am → ~ 1:15 pm.

The meeting didn't go well. I couldn't bring everybody to discussion together. John Esposito want to bring a marker for me, so I could marked what we don't want to do. I felt pretty stupid because I could NOT bring everybody together. Brett was the main speaker. Probably, he did it on purpose because I might have upset him when I asked him question about PEARL vs ARC vs oxynitride ~~on~~ on Tuesday (12/15/98) (n & k a particular = 633? 325nm)

Mike also presented D1261 box plots (BVDSS, Leakage) that D1261 has much higher BD & low/unmeasurable leakage @ 7.5 V because this lot received L-39 resist removed only, oxide & L40/poly were removed by dry etched. Based on this data, Esposito <sup>& the rest of people</sup> said that all we need is a much simpler split than the one presented by Smythe. It came down to split on RTP vs. Deposited oxide for BOE oxide  
RTP oxide for BOE & Dry Etch.

Went to lunch @ Hong Kong

I started working on split list proposed from the morning  
10 am meeting

At ~ 3 pm received priority lists from Mike & Thomas &  
learned that my 1st priority to do Roll-off @ L10 for D1315.  
- D1315 downloaded from hp → RS1

learned from Mike to combine all data into 1 giant table.  
add rows to newtablename from filename\_of\_the\_data

Combined all data into D1315 tablename.

Noticed that wafer 14 has 2

wafer 14 has a lot of bad sites :  $\text{Leftpic (col. 22)} = -2 \times 10^{33}$   
 $\text{Delta L1 (col. 23)} = \text{---}$

(one or two  $\text{Leftpic (col. 48)} = -2 \times 10^{33}$   
bad sites)

Looked Left data, there is not much variation from 1 yfr  
to another. So, I didn't know what I should look at.  
Re roll-off parameters (BVDS, Leakage, etc) against  
And Everybody already gone & give up for today.

- left ~ 6:40 pm

12/24/98, M

- Arrive work ~ 8:10 am
- Attend 8:10 meeting  $\rightarrow$  1<sup>st</sup> priority is to do D1315 L10 roll-off report
- At 8:24 am read emails
- Talked to Mike about what I am suppose to do at the L-10 roll-off. what parameters to look against

\* For L-10 roll-off, the parameters to look at are the same as typical (L40-CD splits) roll-off but against NP-W (= N<sup>+</sup> width).

Typical L-40 CD  $\rightarrow$  Roll-off will be looked at against L<sub>eff</sub> @ L-40

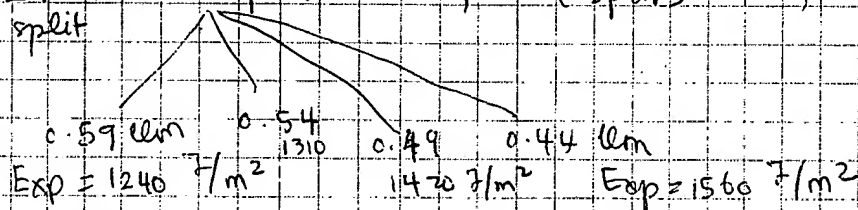
$\rightarrow$  Assume PP-W (= P<sup>+</sup> width) is controlled by the same level as NP-W.

\* Wafers 1-10 received Z37120 process (no capacitors)

wafers 11-25  $\rightarrow$  Z37223 process. The difference between Z37223 vs. Z37120 is the capacitor oxide & poly 2 on Z37223.

\* wfrs: 11-15, 16-20, 21-25  
L10: A, B, C

L40 CD: 4 splits, 4 splits, 4 splits  
split



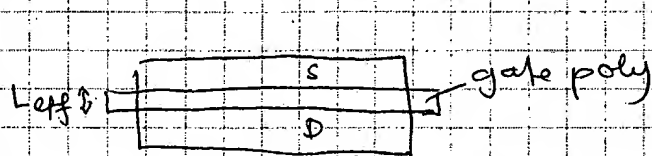
Want to look at wfr 11-15 1<sup>st</sup> to look at L40 CD split  
16-20 2<sup>nd</sup> to  
21-25 3<sup>rd</sup> to

For each L40 CD = f (L10 splits)



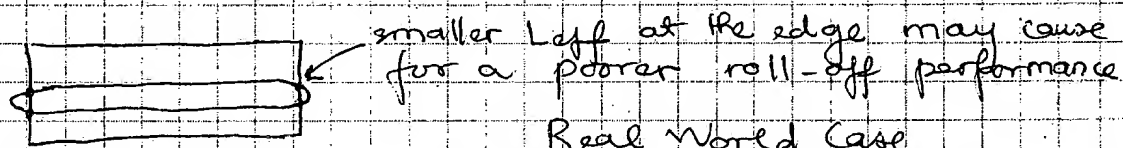
The reason we are increasing  $L_{IO}$  width is because it is thought that the rounding around the edge of the gate causing a poor roll-off performance.

Ideally, we want to have a perfectly uniform & sharp edge of gate.

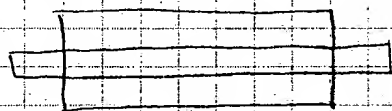


No change in  $L_{eff}$  amount

Ideal case



Real World Case



Pearl layer should take care of the rounding edge effect.

Typically  $n$ -channel poly gate width is compensated from  $0.5 \mu m \rightarrow 0.35 \mu m$

$p$ -channel poly gate width is NOT compensated

strd1315.hp = wafer 1  
strd1315\_a.hp = wafer 2

strd1315\_b.hp = " 3

~~d.1315.hp = 15~~ wafer #

- c.hp = " 4

PERAL  
wfr 10 → 12

- d.hp = " 5 → 6

- e.hp = " 7

- f.hp = " 8

- g.hp = " 9

PERAL retest

- h.hp = " 10/12

12 & 13 are same = 13

- i.hp = " 12/13

make boxplot just 2 from col 3  
to col 3

retest  
some parameters shift

- j.hp = " 13

10 → 12

- k.hp = " 14/15

12 → 13

- l.hp = " 17

W/O OPC → lower Left

- m.hp = " 18

- don't want to use 13  
because it is a  
retest.

- n.hp = " 19 → 20

dis col 8/10/15 =  
where col 13

- o.hp = " 22 → 23

- p.hp = " 24 → 25

strd1315\_q.hp = " 15<sup>14</sup> (use this file)

wfr 11 was pulled after P1-deposition for AFM

wfr 16 was pulled out for AFM analysis (after P1 anneal)

" 21 " " after Capox Deposition for AFM

Wafer 15's data got shifted by 1 col, approximately col 5 → 8.  
Later Lee fixed that, so I don't need to shift it or guess which  
col is for which.

col 3 = VTLEXN\_1

col 29 = VTLEXP\_1

col 11 = VTLENC ✓  
 12 = GMMN\_2  
 13 = GAMMA\_2  
 14 = VTON\_2  
 15 = VTSEXP\_2  
 16 = IOFFN2  
 17 = SN\_2 ✓  
 18 = IDSANC  
 19 = BVDSNC ✓  
 20 = IBSP\_2A  
 21 = DIBLN  
 22 = LeftNC  
 23 = Delta\_L1  
 97 = NP\_W  
 99 = PP\_W  
 1 = wafer

col 36 = VTSPC  
 37 = GMP\_2  
 38 = GAMMA\_P2  
 39 = VTOP\_2  
 40 = VTSEXP\_2  
 41 = IOFFP2  
 42 = SP\_2  
 43 = IDSAPC  
 44 = BVDSPC  
 45 = DELTA\_W2  
 46 = IBSP\_2A  
 47 = DIBLP  
 48 = LEFTPC  
 49 = Delta\_L2

SN\_2 vs. LeftNC VTSENC (km)  
 BVDSNC vs. LeftNC VTLEXP\_1 (V)  
 IOFFNC vs. LeftNC  
 BVDSNC vs. IDSANC  
 VTLENC vs. LeftNC

IOFFN2 has a lot of huge #  $12^7 \rightarrow 12^{11}$  data that I got rid off.  $\Rightarrow$  on wafer #14

SN\_2 & SP\_2 also got rid off data pts =  $1.7e^{33}$

SN\_2 most bad sites occurred for wafer 14  
 There is one (-) # ( $\sim -427$ ) occurred for wafer 15 (SN\_2)

DIBLN has a lot of  $-4e^{30}$  pts for wafer 14

IDSAPC remove  $8e^{10}$  data pts

IOFFP2 remove  $-e^{+7} \rightarrow -e^{+10}$

Through out the day, generating plots from these table:

D1315A (wfr 12-15)  $L_{10} \text{ DICD} = 0.8 \mu\text{m}$ ,  $\text{Exp} = 1600 \text{ J/m}^2$

D1315B (wfr 17-20)  $L_{10} \text{ DICD} = 0.9 \mu\text{m}$ ,  $\text{Exp} = 1450 \text{ J/m}^2$

D1315C (wfr 22-25)  $L_{10} \text{ DICD} = 1.0 \mu\text{m}$ ,  $\text{Exp} = 1200 \text{ J/m}^2$

12/22, Tuesday

- Went to see a physical therapist from 8:15 → 9:30 am
- Arrived work ~ 9:35 → 9:40 am.  
Went directly to the PI-group meeting at 9:30 am until 11 am

From the meeting, I learned these are my priorities:

\* DIBIS L10 / Pearl Split, Lot Report L10 roll-off sensitivity is my 1<sup>st</sup> priority.

Want to resolve SW effective issue. Want to get this issue out of the way.

\* DIBIS Lot Analysis Well Annual is my 2<sup>nd</sup> priority

\* I-V-T on SLM 07 / 09 / 55 (D1114) may be my 3<sup>rd</sup> priority. This is a clean up issue.

Global priority:

1. Lot 1549 → will tell us the unit process of L-40 etch.
2. DIBIS (SV)
3. STR: 7223 IPO Removal STR L39/L40

Tim wanted to go over the split list for L39/L40 STR at 3:30 pm.



The plots generated are

Boxplots  $V_{tlexn-1}$  (V) vs. wafer #  
 "  $V_{texp-1}$  (V) vs. wafer #

VTSEXN\_2 vs.  $L_{effnc}$  (sort = wafer #)  
 BVDSNC vs.  $L_{effnc}$  ( " = " )  
 BVDSNC vs. IDSANC ( " = " )  
 IOFFN2 vs.  $L_{effnc}$  ( " = " )  
 SNL2 vs.  $L_{effnc}$  ( " = " )  
 VTLENC vs.  $L_{effnc}$  ( " = " )

VTSEXP\_2 vs.  $L_{effpc}$  (sort # wafer #)  
 BVDSPC vs.  $L_{effpc}$  ( " " )  
 BVDSPC vs. IDSAPC ( " " )  
 IOFFR2 vs.  $L_{effpc}$  ( " " )  
 SP\_2 vs.  $L_{effpc}$  ( " " )  
 VTLEPC vs. " ( " " )

For each group of L-10 CD, each wafer received L40  
 DICD.  $\Rightarrow L_{10-CD} = f(L_{40-CD})$

- Leave ~ 7:10 pm

- Showed Mike those RS1 plots that I generated yesterday.

The interesting part is that the roll-off (L-40 CD) only occurs for a particular wafer, even-though all wafers (15 → 25) received L-40 D1CD by row.

# - L40 D1CD by row:

0.472

0.425

0.377

0.32

# Loff Targets

0.38 (1)

0.33 (2)

0.28 (3)

0.24 (4)

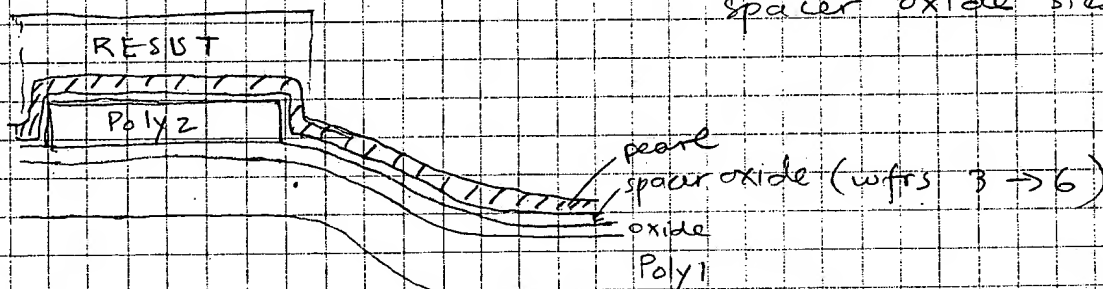
- Generate a Table D1315-L10 to see which set of data for each wafer that received the same L40 D1CD split.

<u>wafer #</u>	<u>split</u>	<u>Loffnc</u>	<u>Loffpc</u>
12	(1)	row 2, 8, 16, 18, 20, 26	
	2	row 4, 6, 12, 14, 21, 23, 29	
	3	row 1, 3, 9, 11, 17, 19,	
	4	row 5, 7, 13, 15, 22, 24, 28	
		<u>row (Loffnc)</u>	
13	1		
	2		
	3		
	4		

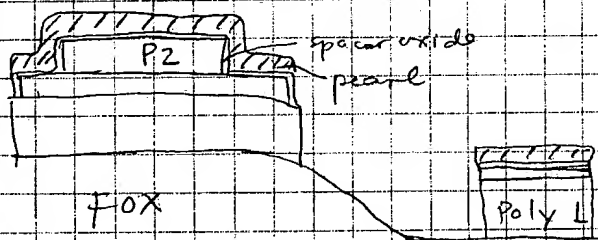
12/23/98, Wed.

- Arrive work ~ 8:15am
- Find a X'mas gift on my chair. It was from David Lee.
- Will work on the split list that Tim & I & Mike discussed about yesterday.

Wafers 1 & 2 do not receive  
spacer oxide step



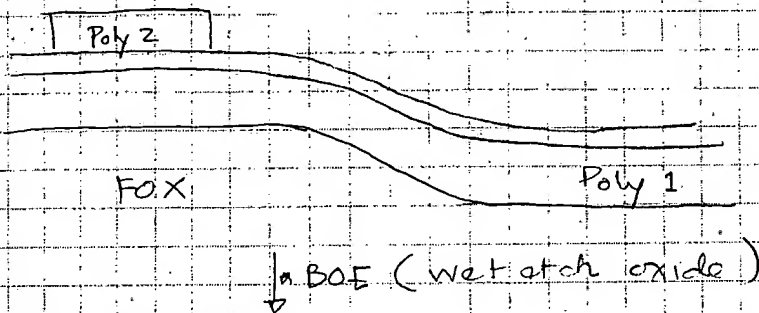
↑ Horizontal  
↓ Etch @ L40  
→ Remove resist



= D1261

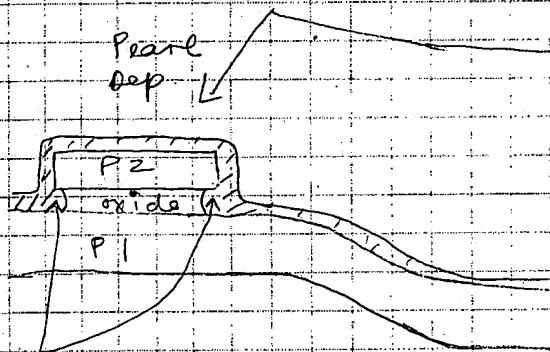
PEARL IS NOT TOUCHING  
BOTH Poly 2 & Poly 1

After L39 mask & poly etch



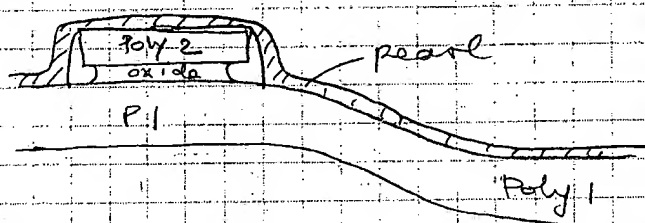
↓ BOE (wet etch oxide)

- \* Spacer oxide (RTP or Dep.)
- \* Etch the top layer of oxide
- \* ↓ Pearl Deposition

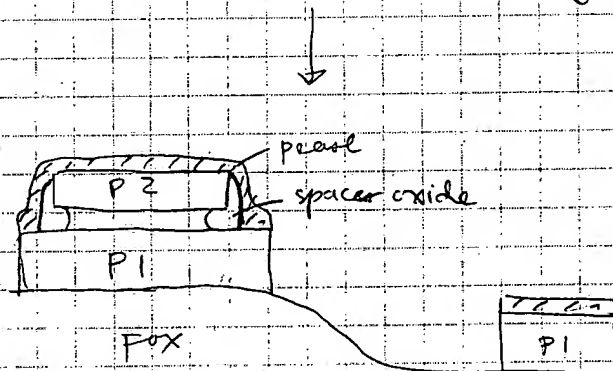
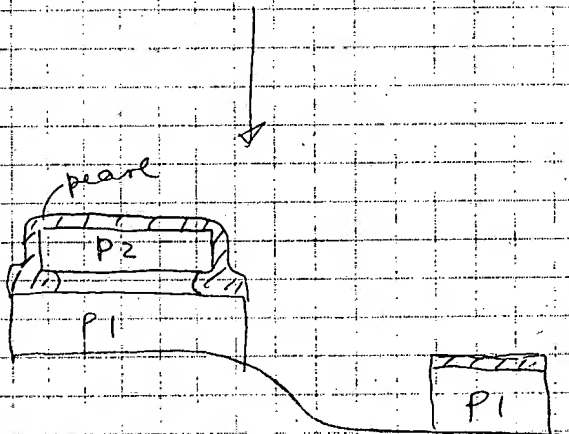


This void could be filled by L39 resist &/or pearl

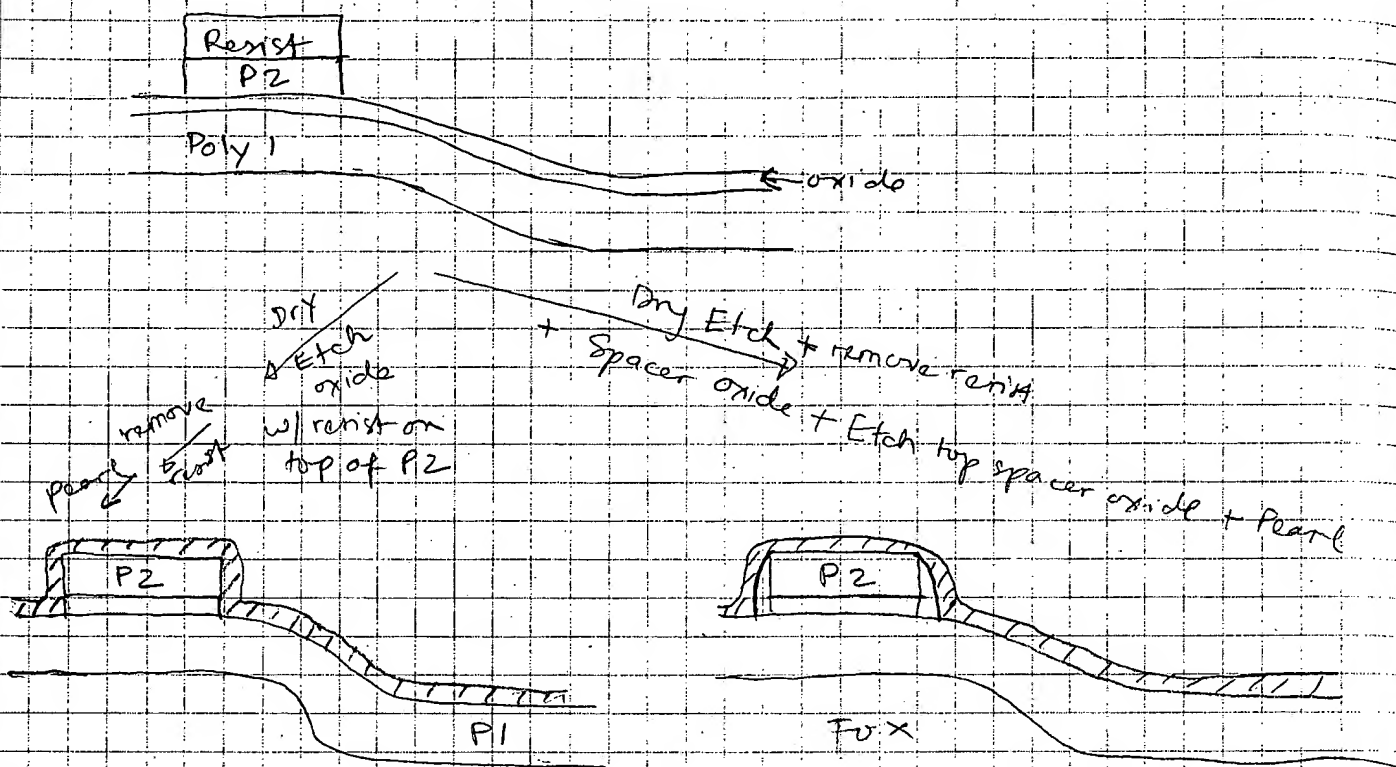
= wafer 7 (= D1114, wfr 2 = thermal wfr 4 = Norvellus)



↓ L40 mask & etch  
would be the same as D1114 (pearl + P1 only)







pearl on both P1 & P2  $\Rightarrow$  may be leakage path.  
 If this is the case then having spacer ox is  
 not going to solve P2 leakage path

dry etch, RTP, 1000 A, 2250 A oxide  $\Rightarrow$  4 possibility of  
 spacer & etch.

12/30/98

\* Went to see a doctor from 8am - 8:45am

\* Arrived work around 9am

\* Meeting @ 9:15 w/ Tim, Thomas, Mike, David & Sunjanti  
- wafer 15, 20, 25 didn't have leakage capacitor problems from D1315 lot.  $\Rightarrow$  have BOE oxide

Pearl contacts both poly 1 & 2  $\Rightarrow$  leakage path

\* \* \* Next year project, current schedule to meet the deadline  
Hit a technology at a time (T223, T235) & see what  
need to be done (at least limited release)  
production > LPR

E37223

L.P.R. = 01-11-99

contingent: ① one lot through

500x temperature cycle, needs:

- wafers
- test program
- final test
- burning <sup>in</sup> board
- STWR

} into qual.  
D1550 will force  
these items to  
get done.

Rubin, Zippi names were mentioned.

We can use D1549 as quality item as well  
as a back-up wafers

D1550 = call it "Qual 1"

D1549 = Qual 2

② Need D1549, data D1315 (capacitor), D1168  
SGIR's STR

Esposito didn't have objection for limited  
release based on several wafers' results

Take capacitor from D1549 & D1315 (wafers  
that don't have undercut w/ pearl) & also  
transistor (L40 split - Loff) data as well.  
But, mostly focus on capacitors

Need lot rep on D1549 & D1315

- ③ D1168 is not on a critical path for limited release based on D1549 & D1315 data

u3 → Need to CN process: Novellus & no densification may still need to work on the type of etching for oxide

D1549 splits are actually as D1261, except D1261 was misprocessed. So D1549 is to repeat D1261.

Need to update PSC 7223 based on D1168, D1315, D1549

- ④ Manufacturing / structural (see Z37223 PSC)

Need to collect L39 data: CD, overlay, cap-ox thickness, poly thicknesses

After D1114 lot → can get CD & overlay data

" " " → poly  $I/I$ , oxide thickness

" D0968 lot → Novellus

Etch issue is waiting for my 1st STR

#### ⑤ Electrical

capacitor/resistor { D1549, D1315  
capacitor matching { Novellus, no undercut & pearl  
whether it structural or measurement issue  
transistor — same for nominal  $I_{eff}$   
need to do # summary w/ Z70 lots

CMA T for undercut / no-undercut  
Final PEVAL verification (9 sites for production)

#### ⑥ Yield

- Sort program & results (D1549 rom code ?)

was D1549 has the same rom code? check it

(7) Reliability Test (mentioned on #1 above partially)

(8) Performance

→ Spice - at least the analog needs to get done  
DIS49 if the thickness is closed

Ring oscillator? (can do it in design review)  
(Esposito) speed is not affected by additional SLMs

full spice for capacitor & resistors are not necessary

who's doing what based on the Z37223 list for  
limited release above:

Z37223:

(2) D1168 lot report & roll-off  
SGIR STR #1 priority (moved to Limited PR list)

(6) Reduce  $V_{pp}$  to 50mV or Cap

(5) CMA-T issue (CMAT CVCO are as important for converter devices)  
D1114 ring oscillator summary (Lee - done)  
WTC 37223

(1) add → D1114 PEVAL

(9) → New SLM verification

Final PEVAL verification (9 sites for production PEVAL)

(1) add → D1261 Review

(Add SLM 272 to PEVAL test (waffle type capacitors w/  
guard ring)  
part of H15

(10) investigate scattering PMOS roll-off

SLM 200 current mirror fix (Scott)

(8) Design rule Margins

FPR = Full production Release (12/31/99)

Deliverables

for good capacitor (high BV  $\approx 15V$ )

(4) capacitor test: RBD, 5V or 7V over some time & temp (stress test)  
characterization



- ③ Bipolar, transistors <sup>matching</sup> & poly 2  
up to this pt, we don't have bipolar result yet.

LPR 2/15/99 → if final test program (is gated by qual)

Z37235 : Z37125, Z37130

Z37235 contains all these 3 technology

FPR on Z37235 depends on L02 (Z37223 FPR date)

④ Product 1<sup>st</sup> Si (90365B, 90233C)

- ① - Need STR signed by Esposito → dated 2/17/99  
if start on 1/4/99 don't have problem meeting the date 2/17/99.

- 90233 PEVAL @ M1, M2, ~~final M3~~ (transistor matching)

⑤ Qual lots

related

- ② supreme simulation (BV + D1315)  
③ HCI D1315 & modify to industrial record (Tower)  
④ D1315 lot report  
⑤ Left resolution (PEVAL / New SLM)  
⑥ 7125 margin analysis (rev. 1)

⑦ PEVAL setup for 90365B / 90233C

caps  
triple layer metals (one PEVAL @ each metal layer) for 90233C.  
TLM  
VT-match

⑧ Isubs reduction → maybe simulation

⑨ Snap back @ 5.5V → ~~6V~~ → 6V (Maric McKencick? ~~Product Eng~~ Eng @ Campbell)  
According to Tim, they pushed it back to 7V

⑩ SRP / simulation correct on final process

⑪ PMOS IOFF

⑫ PPLKG (random is working on this)

Delta W targeting

⑬ PSC structural, y8EMS (metal 3 & planarization steps)



## Z37120

- ⑤ DW targeting (see PSC)
- ⑦ M1/M2 correlation
- ② edit, DO 931 SRP
- edit, HCI characterization
- ③ { final PSC (10 lot PEVAL)  
PEVAL Summary (10 lot)
- ① Deliverables sp
- ④ L10 roll-off rpt for D1315  
L10 fix mod III (NP-W)
- ⑧ I-V-T SLM 07/09/93 on final SLMs  
Diode Leakage mod III
- ⑥ Well-anneal lot report

## Z37229: FLASH - 5V (polycide is part of flash)

- need NTP

We've done chisel cell characterization. We have several work for FLASH. It may not be flash, it may be mid-rom L45 (= enhancement rom, for 3V is not a problem, but for 5V it may be a problem because punch-through is right at the edge)

## Z37126: 3V mid rom (L45 enhancement)

- NTP

## Z37128: 5V mid rom

- NTP

## Z37122: 1.5V core → NTP

go to there because of likelihood for it to work

(polycide?)  
High density SRAM (TV - cache memory for picture in picture)

1-4 Meg, require low power consumption

cell size  $3 \mu m^2$  right now

Most company used SRAM as their goal because of complexity

polycide - D NTP & a working ring oscillator compactness & # of fail sites

Z37229, Flash 5V

- NTP → flow, financial, PSC rev.00, DR 0.0, margins
- test chip (Pete Manos)
- Need the most development (#1)

Z37126 } - tape out  
Z37128 } - 02-99

#5

- NTP
- BVDS simulation for enhancement device; see if 3V, 5V are sufficient

~~Z37122~~ High Density SRAM (polycide?) , 03/99

- NTP
- Test chip
- industry review (see what's out there?)
- #2

Z37122 : 1.5 core, completion / tape out year 2000

#4

Salicide - #3 development

- Set up a meeting for reviewing the Z37223 experiment L39 / L40 on 1/4/99 afternoon. Key players: Esposito, Smythe & Carns. Do the L-10 DISIS report 2<sup>nd</sup> priority 1/13/99
- Shoot for limited production release on 1/15/99 based on the data up to DIS49 data.
- Capacitor characterization 1/13 - 1/25/99 (3<sup>rd</sup> priority)
- Capacitor matching - Mike does this  
the HP4146 doesn't have the resolution to measure capacitor matching. So Mike will need Lee's help to use PEARL system.

\* Update the split list

- L40 Etch:

A : Pearl(325A) + Oxide + Poly 1

wfr 1 & 2

PEARL 325  
oxide 375  
Poly 1

B : Pearl(325A) + Oxide (~500A)  
+ Poly 1

wfr 3

Pearl 325A  
oxide ~500A  
Poly 1

C : Pearl(325A) + Poly 1

4, 5, 6, 7, 8  
10, 11, 12, 13, 14  
16, 17, 18, 19, 20, 21

Pearl 325  
Poly 1

D: Pearl (325A) + oxide (~200A) +  
Poly 1

wfr 15

Pearl 325  
oxide 200

Poly 1

E: Pearl (800A) + oxide (375A) +  
Poly 1

wfr 22

Pearl (800)  
oxide (375 A)

Poly 1

F: Pearl (800A) + Poly 1

wfr 23

Pearl (800 A)

Poly 1

G = Poly 1

wfr: 24, 25

Poly 1

no undercut w/ pearl → will show leakage  
13 & 14

9-12 with undercut, spacer might help & leakage

wfr 24 works, by default wfr 25 will work

22 - line width variability  
800A pearl

\* Printers problem. Can not print out to all printers

\* Edited the D1114 Pearl summary / Lot report, gave it back  
to Tim ~ 6:15 pm electronically

\* Left ~ 6:30 pm



12/31/98, "Th

\* Arrive work ~ 8:05 am

\* No meeting today because Fab is down & Bob Acock is not here. All of the unit process engineers & mod 3 engineers are off from Christmas till Jan 4.

\* Start working on the run-card for L39-oxide-L40 split list.

Mostly in the morning, downloading the runcards (Z37120 & Z223) from public folders. Inserting Z37223 process flow to Z37120.

Learned from Mike, how to eliminate the huge page number from the runcard. It is under: View  $\rightarrow$  Normal.

\* Tim came by & told me that I sent him the wrong version of D1114 summary file (from last night), so I resent him the correct version.

About 1 hr later, he signed off the D1114 summary report. I copied the report, gave the original to John Smythe (Ask security to open his office - to drop off the report).

\* Went asking Mike about any suggestion preference to change # of wafers for a particular split of L39-oxide-L40 proposed splits. He said no preference. Then, Mike said, <sup>doesn't</sup> he thinks the proposed <sup>split</sup> will completely answer our questions: that is from D1315, we know wafers 15, 20 & 25 that DID NOT receive PEARL, but w/ undercut below poly 2, perform well, leakage is ~ 3 orders of magnitude lower than the rest of wafers 1-14, 16-19 & 21-24 that received pearl.

So, Even w/ undercut of oxide below poly 2 & NO Pearl, the capacitor's leakage performed well. Undercut & pearl result in poor capacitor leakage. This means pearl acts as an ~~of~~ the leakage path.

(resist strip only) Initially D1315 split list and run-card were designed to have NO OXIDE Removal @ L-39. But the run-card from the fab shows that all D1315 wafers received BOE oxide removal @ L39 (IPO Removal). This action was probably taken after they found out a large swing (0.01-0.02  $\mu$ m) in Loff caused by having oxide below pearl from D1261 & D1549 lots. 4.



# 87L02 CAPACITOR OXIDE SPLIT

Wafer #	Capacitor Oxide (wait for data from D1549)	L39 IPD Removal	Cap. Spacer Oxide	Pre-clean	Capacitor Spacer Oxide Thick (A)	Spacer Etch	Pearl Deposition	L40 Etch	L40 D1CD Splits	Hook Wafer
1, 2	Novellus	---	---	---	---	---	Y (325A)	A	Y	D1261: 18-20 D1549: 8 & 18
3	Novellus	---	RTP	---	---	---	Y (325A)	B	Y	
4	Novellus	---	RTP	---	---	A	Y (325A)	C	Y	
5, 6	Novellus	---	DEP	Y	1000	B	Y (325A)	C	Y	
7	Novellus	---	DEP	Y	2250	C	Y (325A)	C	Y	
8	Novellus	BOE	---	---	---	---	Y (325A)	C	Y	D1114-4
9	Novellus	BOE	RTP	---	---	---	Y (325A)	D	Y	
10	Novellus	BOE	RTP	---	---	A	Y (325A)	C	Y	
11	Novellus	BOE	DEP	Y	1000	B	Y (325A)	C	Y	
12	Novellus	BOE	DEP	Y	2250	C	Y (325A)	C	Y	
13, 14	Novellus	Dry Etch	---	---	---	---	Y (325A)	C	Y	
15	Novellus	Dry Etch	RTP	---	---	---	Y (325A)	D	Y	
16, 17	Novellus	Dry Etch	RTP	---	---	A	Y (325A)	C	Y	
18, 19	Novellus	Dry Etch	DEP	Y	1000	B	Y (325A)	C	Y	
20, 21	Novellus	Dry Etch	DEP	Y	2250	C	Y (325A)	C	Y	
22	Novellus	---	---	---	---	---	Y (800A)	E	Y	
23	Novellus	Dry Etch	---	---	---	---	Y (800A)	F	Y	
24	Novellus	BOE	---	---	---	---	N	G	Y	D1315-15
25	Novellus	Dry Etch	---	---	---	---	N	G	Y	

Spacer etch is a blanket etch → open etch

Main objective of the proposed splits

Minimal process modification from Z-70 process flow.

Questions to be answered:

Poor leakage capacitor performance on SLM 270 and emission around the edges of capacitor from hypervision experiment suggest that we have the following possibility of leakage path:

1. Undercut of capacitor oxide using BOE. This issue is investigated by implementing spacer oxide (RTP vs. DEP—1000 vs. 2250 Å), dry/wet etch oxide and/or not removing oxide at L39.
2. Contamination of Pearl and capacitor oxide in undercut region. This issue is investigated by implementing spacer oxide step and not removing oxide at L39.
3. Pearl layer touching both poly 1 and poly 2. This issue will be resolved by not removing the oxide at L39.

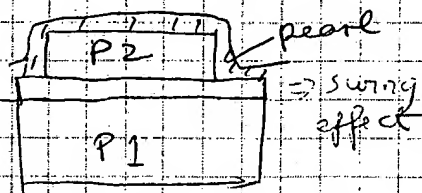
The swing effect remains on the wafers that receive no oxide removal step. This effect is also investigated in the proposed splits:

1. By increasing pearl layer thickness to 800Å. This step requires some photo and CMP development.
2. By eliminating pearl layer. This step will reduce the line width control of L40.

Note for L40 Etch:

- A = Pearl (325Å) + Oxide (375Å) + Poly 1  
B = Pearl (325Å) + Oxide (~500Å) + Poly 1  
C = Pearl (325Å) + Poly 1  
D = Pearl (325Å) + Oxide (~200Å) + Poly 1  
E = Pearl (800Å) + Oxide (375Å) + Poly 1  
F = Pearl (800Å) + Poly 1  
G = Poly 1

Mike is thinking about patterning some steps that have oxide ~~pad~~ to prevent pearl from touching both Poly 1 & 2, yet ~~not~~ reducing / eliminating the swing effect @ L40 (caused by pearl on oxide) → poor line-width control @ L40.



D1261 & D1549

cost effective  
easy to implement  
improvement of certain factor

These 3 factors were in our conversation around noon: like what kind of steps one has to take to pattern an idea. It is not necessary to convert the idea to a practice. In other words, it is not necessary to have experimental data to support your idea.

According to Mike, if he has an idea, he would file an ~~in~~ invention disclosure form & put his name on it. From places that he has worked, some people would go around asking questions about what he/she thinks about how to resolve a problem & then file a pattern that wasn't even his/her own idea. So, want to be careful & discrete when asking questions that might be helpful to your idea w/o disclosing your idea.

(18)

Typical turn around time to have a bonus from an idea that accepted into a pattern is about 1-2 years. During this time if you get laid off, quit or fired, you won't receive the bonus (18) likely.

Generally, after you file an invention disclosure form & submit a few pages that describe when & how you came out w/ the idea + other details, it gets sent to corporate office & review by a lawyer to see if it is worth patterning or to check if the idea has been used. Then the lawyer will rewrite your original idea to cover as many possibilities as possible w/ legal binding to it & resend it back to you to review. At this pt, you won't even recognize the original report you wrote, but the basic idea is there. Then, once you approved it, send it back to the lawyer, & the lawyer will send it to pattern office. If accepted, you will get from ~\$500 → \$1,000 / pattern.

From our lengthy conversation about patterning an idea, suddenly the idea to reduce the oxide under-  
neath pearl layer struck my mind.  
Suddenly, I started thinking about the basic optical properties of pearl film on oxide.

I told Mike that I do not <sup>know</sup> what  $\lambda$  (wave length) they use @ L-40 exposure. I know it is UV light, but don't know exactly @ what  $\lambda$ . Also, at what

$\lambda$ , pearl layer ~~is~~ starts absorbing the light. <sup>similarly</sup> Interaction of light to pearl & oxide film. <sup>for the oxide</sup> How light changes phase @ every interface & interferences affect, etc.

They are many things <sup>optically</sup> that I don't know @ this pt.

But it sure sounds like reducing the oxide thickness down to 20 - 50 Å might reduce the swing effect, yet provide the insulation of pearl from poly 1 & 2.

So, Mike suggested that I discretely ask this question to Brett Lowe.

The preferred technique to etch the oxide is dry etch, although BOE might work too.

We leave it at this pt, right now. I definitely will find out more about the rate of success for this idea later.

We also talked about the possibility of using oxynitride as the alternative mtl ~~to~~. The difference between pearl & oxynitride is different growth condition in the same chamber. pearl is Si-rich w/ some  $O_2$  &  $N_2$ . Oxynitride is NOT Si-rich.

If oxynitride has been used by some-else for line-width control ~~at~~, then ~~the~~ oxynitride may be another option.

If it has NOT been used, need a lot of development.

\* The rest of afternoon, worked on the run-card based on the split list in previous page.

Obtained the exposure & D1CD values from Mike @ ~5:35 pm

The values used are the same as <sup>the ones used in</sup> D1315 for L40 - D1CD split.

Got the general / most run-card done.

\* Send out emails to plan a meeting to review an SDE on 1/4/99 at 2:30

\* Left - 6:10 pm



1/3/99, Su

- Came to work around 4 pm
- Answered personal emails
- Printed out 1999 calendar
- Work on minor details (line, cell alignment, size of font, etc)  $\Rightarrow$  then printed out the run-card
- Wrote down what I did on 12/31/98.

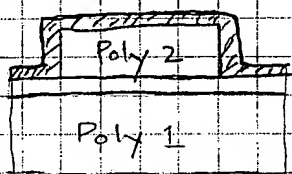


1/4/99, M

- \* Arrive work ~ 8:10 am
  - \* Attend Monday meeting
  - \* Send out email to inform the location for meeting at 2:30 pm today. It is going to be in blue-room.
- I invited: Tim Carns, M. Westphal, Lee DeStuler, John Esposto, John Smythe, Pee Kiebel, Min Huang, Jon Daley, John Horvath, Mitch Mooney, Brett Lowe, Jim Sheu, John Gdd & Steve Buffat.

- \* Will work on SDE presentation (see split list on 12/31/98)

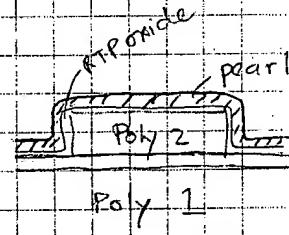
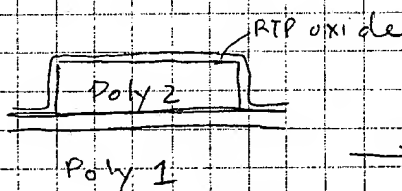
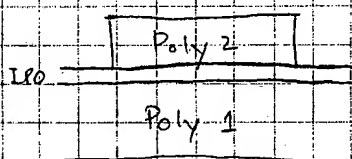
Wafer 1 & 2



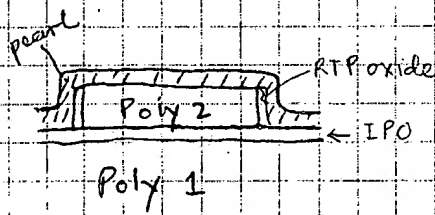
Poly 2 is defined at L39  
oxide & poly 1 are defined at L40

L40 etch removes pearl (325 Å) + oxide + poly 1

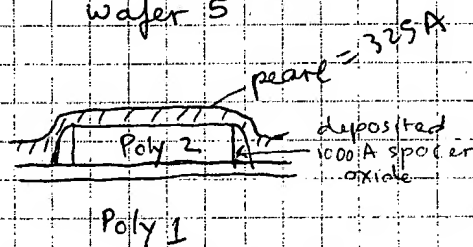
wafer 3



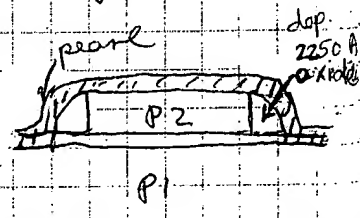
wafer 4



wafer 5



wafer 6



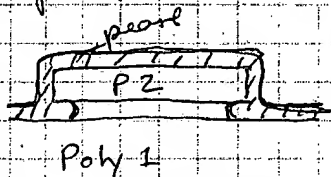
wafers 1 → 6 : Pearl does not contact both P1 & P2 at the same time

structure  
We knew this<sup>n</sup> will dramatically improve capacitor performance (D1261 & D1549). But swing effect at L40 arises by having pearl on oxide.

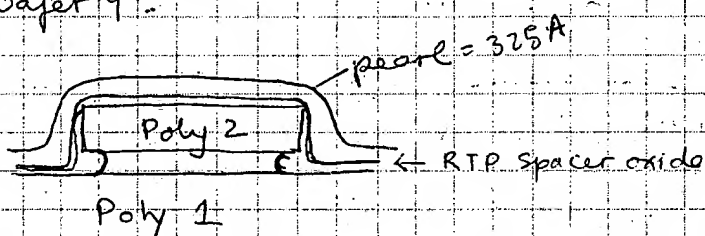
Wafers 1-6 will also tell us whether swing effect @ L40 will get worse or better by having thicker oxide underneath pearl.

Wafers 8  $\rightarrow$  12 : Novellus oxide & BoE at L39  
Pearl contacts both poly 1 & 2.

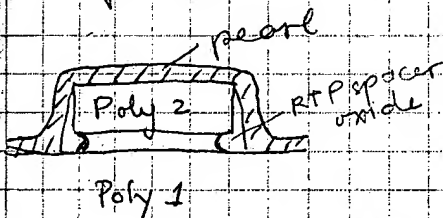
wafer 8:



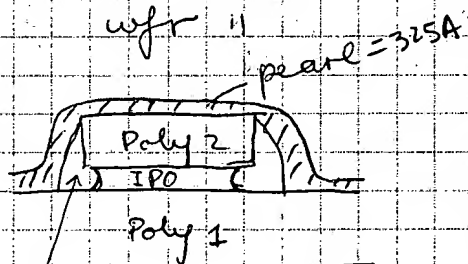
wafer 9:



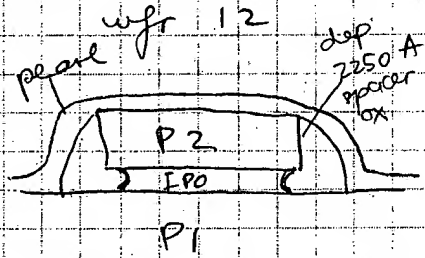
wafer 10



wafer 11



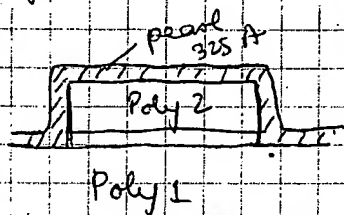
wafer 12



wafers 13  $\rightarrow$  21

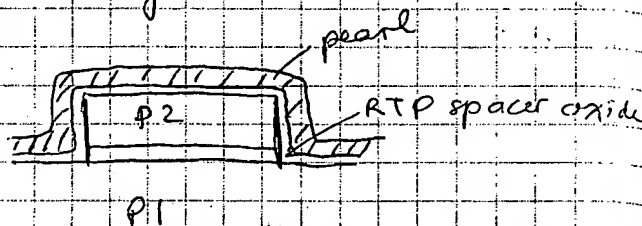
Novelty capacitor oxide, dry etch IPO removal

wfrs 13 & 14



Pearl touches both P1 & P2

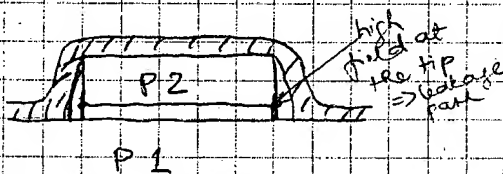
wafer 15



RTP spacer oxide provides as an insulation for pearl to contact both P1 & P2

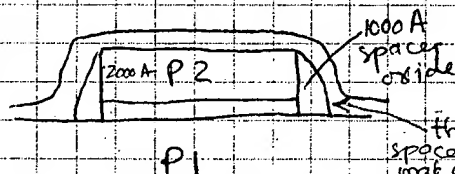
wfrs 16 & 17

RTP spacer ox & then etched



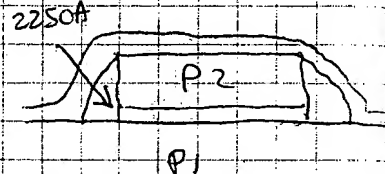
wfrs 18 & 19

1000 Å dep. sp. oxide



wfrs 20 & 21

2250 Å dep. sp. oxide



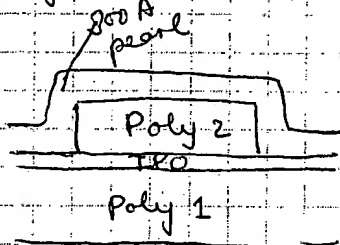
For the wafers where pearl touches both poly 1 & poly 2, the spacer might help reducing the leakage path, but capacitor performance is not optimized because pearl is the leakage path.

Initially without spacer (wfrs 13 & 14), IPO thickness  $\sim 375$  Å.

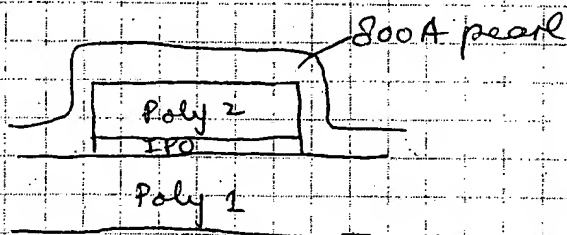
Later, with spacer (wfrs 16  $\rightarrow$  21), the total leakage path is longer (from 375 Å = IPO to  $\sim 3750$  Å). So the leakage path thru pearl is longer, which may improve or reduce cap-leakage by  $\sim 1$  order of magnitude assuming linear relationship of the oxide thickness to the leakage. But, again the capacitor performance is not up to its max as long as pearl touches both poly 1 & poly 2.

\* wfrs 22 & 23 : Novellus oxide & 800 Å pearle

wfr 22 : No IPO Removal @ L39

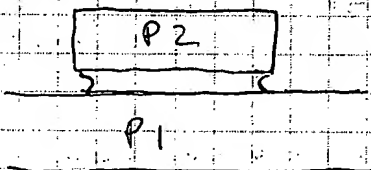


wfr 23 : dry etch oxide

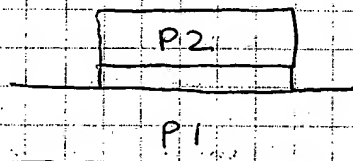


wfrs 24 & 25 : Novellus cap. oxide, BOE vs. Dry Etch, NO PEARL

wfr 24, BOE



wfr 25, dry etch





\* \* Meeting @ 2:30 - 3:30 pm to review an SDE for capacitor (L39-oxide - L40)

Here is the proposed splits, more or less reflect our discussion from last year (a few wks ago). The objective of the splits is to answer the leakage path, whether it is caused by undercut oxide using wet etch (BOE), contamination of pearl and oxide in undercut region, or pearl touching both poly 1 & 2. @ L40 due to pearl on oxide

The swing effect is also investigated in this split.

This split was <sup>initially</sup> proposed before having D1315 data which show pearl layer contacting both poly 1 & 2 acts as the leakage path even w/ undercut oxide

Correction at L-40 etch was made for wafers 4 - 7. This correction was printed out by Jim Shen

With that, the floor is open for discussion, comment, suggestion or objection that all of you have

Attendees: Deb Acock, Jean Adams, Steve Buffat, John Horvath, Bee Kicket, J. Smythe, T. Carrs, M. Westphal, Mitch Mooney, Shelly Dove & L. Debnuler

The meeting went pretty well, although it seems that there is a need to go over the split, by ~~split~~ <sup>objection</sup> column to the audience, even though the split list <sup>objection</sup> was already sent out to them w/ the meeting notice.

There is ~~almost~~ no objection. D1315 data was also presented i.t. of leakage 270 vs. wafer # where the boxplot shows all wafers (15, 20 & 25 having no pearl & no OPC) have several order of magnitude lower in leakage value than wafers that received pearl & OPC. Tim wants Mike to present that data on Wednesday (1/7/99).

There are some minor changes on the split list, see next page.

After meeting, Tim wants to go over the run-card w/ J. Horvath, M. Westphal, J. Smythe, B. Kicket & Deb Acock. I told him that I can get the run-card done in ~ 1 hr w/ the right wafer #.



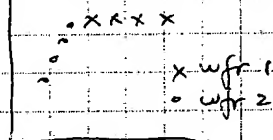
\* Send out another meeting notice to invite those people to review the run-card @ 4:15 pm in Blue room to review run card for the split list presented a few hrs earlier. All came, except Bee who later drop by briefly to talk to Deb Acock.

- At this meeting, additional experiment is added: The effect of dry resist strip vs. no dry strip at L39 for IPO removed w/ BOE & dry etch techniques (wafers 18 & 12; 20 & 21 → see the attached split list on next page).

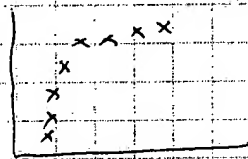
- Tim also wants me to plot  $\text{Leff}$  by exposure for different splits; for D1315 lot: pearl vs. no pearl; for D1549 by different L40 etch. This plot will determine the exposure & D1CD for L40 in the new p STR. (my 1<sup>st</sup> STR).

Want all wafers to have  $\text{Leff}$  in non-roll off & roll-off region.

In D1315, we have most wafers (11-25) data in non roll-off region; only the ones that receive no pearl shows roll-off region w/ no data in non-roll off region.



So, we want this, no wafer has data in roll-off & non-roll off region:



- No PEVAL @ M1

- Attach PEVAL sheet to the run-card, ask Lee about this

- J. Smythe, Re RPP spacer oxide thickness is  $\sim 50 \text{ \AA}$ . I am glad to hear this because this 50A may be enough to provide an insulation for pearl from contacting both polys. Although my initial idea was not growing any spacer oxide, it was to use the IPO & etch it slightly incomplete to leave  $\sim 20\text{-}50 \text{ \AA}$  of oxide on poly 1. But this might work too.

w/spacer oxide

\* From ~5:15 → 7:30 pm  
Make changes on the run-card & split list.

I also talked to Mike about my temptation to try thinner oxide (instead of completely removing it or leave it there).  
So I change the wafer # to have 2 wafers on Novellus,  
Dry strip & dry etch, RTP (spacer oxide), no spacer oxide  
etch, pearl (325A).

\* From run-card review (2<sup>nd</sup> time: Tim, John, Bob & I, Bee  
couldn't make it because of 1:15 pm design review meeting),  
- I learnt from Smythe that white space in L02 with  
waffle's space is as big as L88 chip.

- punch-through step @ L40 Etch is designed to remove 100 Å  
+ 325? 375 Å oxide.

87L02 CAPACITOR OXIDE SPLIT

Wafer #	Capacitor Oxide	L39 IPD Removal	Cap. Spacer Oxide	Pre-clean	Capacitor Spacer Oxide Thick (A)	Spacer Etch	Pearl Deposition	L40 D1CD Splits	L40 Poly Etch	Hook Wafer
1	Novellus	---	---	---	---	---	Y (325A)	Y	A	D1261: 18-20 D1549: 8 & 18
2	Novellus	---	RTP	---	---	---	Y (325A)	Y	B	
3	Novellus	---	RTP	---	---	A	Y (325A)	Y	A	
4	Novellus	---	DEP	Y	1000	B	Y (325A)	Y	A	
5	Novellus	---	DEP	Y	2250	C	Y (325A)	Y	A	
6	Novellus	Dry Strip, BOE	---	---	---	---	Y (325A)	Y	C	D1114-4
7	Novellus	Dry Strip, BOE	RTP	---	---	---	Y (325A)	Y	D	
8	Novellus	Dry Strip, BOE	RTP	---	---	A	Y (325A)	Y	C	
9	Novellus	Dry Strip, BOE	DEP	Y	1000	B	Y (325A)	Y	C	
10	Novellus	Dry Strip, BOE	DEP	Y	2250	C	Y (325A)	Y	C	
11, 12	Novellus	NO Dry Strip, BOE	---	---	---	---	Y (325A)	Y	C	
13, 14	Novellus	Dry Strip, Dry Etch	---	---	---	---	Y (325A)	Y	C	
15, 16	Novellus	Dry Strip, Dry Etch	RTP	---	---	---	Y (325A)	Y	D	
17	Novellus	Dry Strip, Dry Etch	RTP	---	---	A	Y (325A)	Y	C	
18	Novellus	Dry Strip, Dry Etch	DEP	Y	1000	B	Y (325A)	Y	C	
19	Novellus	Dry Strip, Dry Etch	DEP	Y	2250	C	Y (325A)	Y	C	
20, 21	Novellus	NO Dry Strip, Dry Etch	---	---	---	---	Y (325A)	Y	C	
22, 23	Novellus	---	---	---	---	---	Y (800A)	Y	E	
24	Novellus	Dry Strip, BOE	---	---	---	---	N	Y	F	D1315-15
25	Novellus	Dry Strip, Dry Etch	---	---	---	---	N	Y	F	

## 87L02 CAPACITOR OXIDE SPLIT

Main objective of the proposed splits

Minimal process modification from Z-70 process flow.

Questions to be answered:

Poor leakage capacitor performance on SLM 270 and emission around the edges of capacitor from hypervision experiment suggest that we have the following possibility of leakage path:

1. Undercut of capacitor oxide using BOE. This issue is investigated by implementing spacer oxide (RTP vs. DEP—1000 vs. 2250 Å), dry/wet etch oxide and/or not removing oxide at L39.
2. Contamination of Pearl and capacitor oxide in undercut region. This issue is investigated by implementing spacer oxide step and not removing oxide at L39.
3. Pearl layer touching both poly 1 and poly 2. This issue will be resolved by not removing the oxide at L39.

The swing effect remains on the wafers that receive no oxide removal step. This effect is also investigated in the proposed splits:

1. By increasing pearl layer thickness to 800Å. This step requires some photo and CMP development.
2. By eliminating pearl layer. This step will reduce the line width control of L40.

The effect of dry resist strip vs. no dry strip at L39 is also investigated for IPO removed with BOE and Dry Etch techniques.

Spacer Etch:

A = ~50Å RTP Spacer Oxide

B = 1000Å Deposited Spacer Oxide

C = 2250Å Deposited Spacer Oxide

L40 Etch:

A = Pearl (325Å) + Oxide (375Å) + Poly 1

B = Pearl (325Å) + Oxide (~425Å) + Poly 1

C = Pearl (325Å) + Poly 1

D = Pearl (325Å) + Oxide (~50Å) + Poly 1

E = Pearl (800Å) + Oxide (375Å) + Poly 1

F = Poly 1



1/5/99, Tuesday

- Arrive work ~ 8:15 am
- Read emails, no mail
- Write down the stuff I did from yesterday afternoon
- work on the split list, mainly to arrange wafers # accordingly
- Update / change the run-card
- Attend PI 9:30 meeting in West conference room → 11 am
- Ask Tim about the wafers (Loc. 630 L39 cap etch) that do not receive dry resist strip, the resist removal step is included in the IPO removal BoE step.
- update the run-card & STR (ask Wendy how to edit run-card: use Query, type in serial #, hit escape, hit update, this will bring you to edit mode — once added information is typed in, hit escape, then Table to bring to 2nd table, Query, serial #, escape, update, etc.)

Got all of this done ~ 3pm

Will work on plotting  $\text{Leff}$  vs. exposure

→ In this PI meeting, Tim mentioned that we are going to use SRAM chips as our test chip for all future development products. Because SRAM is the most restricted device in terms of size, etc & thus performance ~~is~~ to determine how well our design, device & processes are.

Basically, using SRAM will tell us the worst case scenario <sup>memory</sup>

Tim also presented several future road-map. I wrote down a few:

FLASH: John

Mask ROM converts to FLASH

How many ROM parts would be converted, if any?

Z37123/8/ (3V/5V Lata ROM - L45) Tim

L45: contact mask

L50: define contacts for the ones used & the ones not used get knock off.

Salicide John

1. do we have any products requiring high speed?
2. what is the current maximum speed capability for Z37120 & Z37125 (50 MP/s, 70 MP/s, ??? or more)

MP/s = million per second

3. Will this be necessary for high density SRAM?

Non-volatile testchip


CMOS

Analogy

ETB?

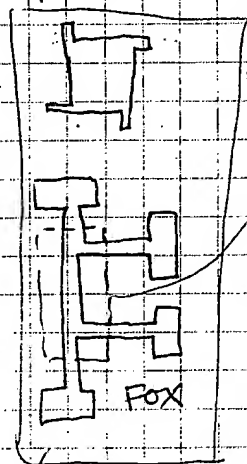
Difference between  $P2\_W\_05$  vs.  $L_{eff}$  per Mike W.:

$P2\_W\_05$  = physical gate width, electrically determined poly line-width

 van-der Pauw to determine sheet  $P$  to calculate  $P2\_W\_05$

$L_{eff}$  = channel length under the gate

$P2\_W\_05$  &  $L_{eff}$  are measured from separate SEM.

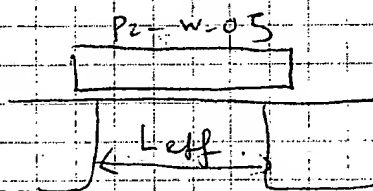


1 SEM

$P2\_W\_05$  is measured on field-oxide. Other company / other device may measure  $P2\_W\_05$  on active area

poly on active area to determine  $P2\_W\_05$  variation from the bottom of active area to the top.

$L_{eff}$  is measured from transistor (during SEM)



DICD -  $L_{eff} = 0.09 \mu m$

0.1  $\mu m$  spec window off from roll-off  $L_{eff}$  from D1114

Because of new - rom code which has NO waffle, poly etch would be etched differently

DIS49 hp files :

strd1549  
 strd1549\_a  
 strd1549\_b  
 strd1549\_c  
 strd1549\_d  
 strd1549\_e  
 -f  
 -h  
 -i  
 -j  
 -k  
 -l  
 -m  
 -o  
 -p  
 -q  
 -r  
 -s  
 -t  
 -u  
 -v  
 -w  
 -x

wager #

1  
 2 & 3  
 4 & 5  
 6  
 7  
 7 (suppose to be 7), but in hpfile it is 8  
 8 & 9  
 10  
 11  
 12  
 13  
 14  
 15  
 16  
 17  
 18  
 19  
 20  
 21  
 23  
 22  
 24  
 25

\* generate a table w/ all of the hp files in col 1

\* to generate a giant table that contains all of the hp files, do this command in RS1

# build ("tablename", col#, "new tablename")

example:

# build ("hpfiles", 1, "DIS49all")

RS1, the peral file  
 col # = REVAL hpfiles

strd1549\_e

8

want to

strd1549\_e

7

8

change 8 to 7 for strd1549\_e

7

do this command @ RS1

strd1549\_f

8

9

Set col 1 where col # = "strd1549\_e" to 8

or

Set col 1 where col # = "strd1549\_e" and col 1 = "7" to "8"

or

# L40 DCD splits

D1315

Exposure	DICD Target	Leff Target	Actual DICD (wfr13)
1500	0.472	0.382	0.486; 0.46; 0.468
1650	0.425	0.335	0.431; 0.418; 0.447
1975	0.377	0.287	0.371; 0.359
2290	0.32	0.23	0.307; 0.315

D1549

Exposure ( $J/m^2$ )	DICD Target	Actual DICD
1500	0.472	17: 0.457; 0.45 18: 0.473; 0.462 0.477; 0.494
1650	0.425	0.441; 0.459 0.429; 0.428 0.393; 0.359
1975	0.377	0.371; 0.363 0.376; 0.352
2290	0.32	0.32; 0.31 0.32; 0.299

wfr 17 & 18

Set: 1500  $\rightarrow$  DICD  $\approx$  0.45

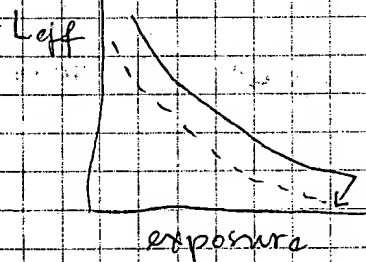
1650  $\rightarrow$  0.38 < DICD < 0.45

1975  $\rightarrow$  0.34 < DICD < 0.38

2290  $\rightarrow$  DICD < 0.34

$\rightarrow$  Set col 7 where col 3  $\geq$  0.38 and col 3 < 0.45 to "1650"

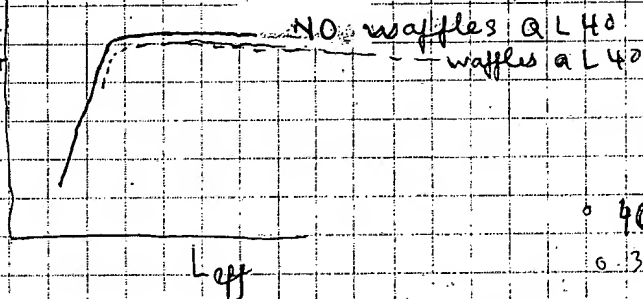
Anticipated Leff behavior by changing L40 mask (waffle & non-waffles)



$$DICD - Leff = 0.09 \text{ um}$$

because of a new rom code which has non-waffle at L-40, Re poly (at L40) will get etched differently  $\Rightarrow$  lower Leff

roll-off curve  
whatever parameter



DICD  
0.472  $\rightarrow$

$\geq 0.48$   
0.40 - 0.45 1960  
0.34 - 0.39 0.40 2190  
 $< 0.35$

\* Leff  $\sim$  8 pm



1/6/99, Wed

- Arrive work ~ 8:10 am
- Read & send emails

- make  $L_{eff}$  vs L40 exposure,  $L_{eff}$  vs  $peval/opc$
- D1315 plots } poly-line width vs. L40 exp, polywidth vs.  $peval/opc$

$$D1C0 = L_{eff} + 0.09$$

$$0.472 - 0.09 = L_{eff}$$

Target

$$L_{eff} = 0.382$$

$$Exp = 1500$$

$$Exp = 1650 \quad L_{eff} = 0.335$$

$$= 1975 \quad L_{eff} = 0.287$$

$$= 2290 \quad L_{eff} = 0.23$$

$$0.472$$

$$0.09$$

$$0.382$$

$$0.32$$

$$0.09$$

$$0.23$$

$$0.425$$

$$0.09$$

$$0.335$$

$$0.377$$

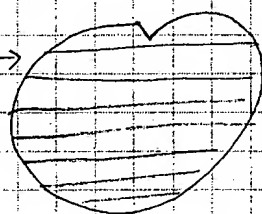
$$0.09$$

$$0.287$$

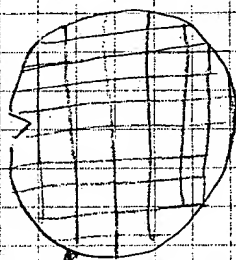
D1315

L40 exposure

row →



PEVAL



row

column

(1, 2)